CHAPTER 3

VOLTAGE SOURCE CONVERTER AS A STATCOM

3.1 Introduction

Benefits of reactive power compensation are well known: increased stability, increased transmission capacity over existing lines, better voltage profile and decreased losses. As it has been mentioned in chapter one, the management of reactive power by traditional means has its drawbacks, depending on compensation technique used. These include a possibility of resonance, slow response, introduction of harmonics, rotational instability or management of reactive power in discrete steps. Moreover, if capacitor banks are used (with or without thyristors), they occupy a considerable amount of real estate. The new generation of static compensator based on converter circuits can successfully overcome those problems and allow reactive power compensation without using bulky capacitors. Unfortunately, the voltage rating of semiconductor switching devices is not high enough for high voltage application. To cope with this problem, a few switching devices must be put in series, or different multilevel topologies are to be used. Multilevel topologies have their advantages over simply putting switching devices in series. These include a better output voltage waveform while FFM (fundamental frequency modulation) switching strategy is used so that filters can be avoided and switching losses decreased. Voltage stress dv/dt in the switching devices is limited to one level of voltage so that converter rating can be increased, allowing direct coupling with AC system without step up transformer. However, the application of power electronic converters are suited to distribution bus voltages and sizes. This is because they are based on solid-state technologies, which have grown from the application of thyristors, gate-turn-off thyristors (GTOs) and insulated gate bipolar transistors (IGBTs) to variable speed AC motor drives. The controllers of SVS such as the Static VAR Compensators (SVCs) and the STATic COMpensator (STATCOM), are solid-state switch technologies pushing upwards to the

higher MVA ratings of power utilities. In fact, this has been one motivation of multi-level converter research. Some manufacturers have already mastered the technology of connecting GTOs or IGBTs in series to increase the voltage ratings of STATCOMs to distribution voltage levels so that they can now be connected directly, without transformers, to the electric utility[47,48].

In this chapter a review of STATCOM principles are presented. The original STATCOM control strategies for voltage control of power system is tailored and tested. Numerical simulation using Hypersim is used to validate proposed control strategy. The positioning of the STATCOM in transmission line is discussed too.

3.2 Voltage Source Converter

STATCOM is basically AC voltage source behind the reactance as illustrated in Fig.6. Voltage source converter (VSC) is used as a voltage source. Fig. 14 a) illustrates one converter leg of basic three phase converter circuit and Fig.14 b) illustrates three phase six pulse converter topology. The VSC is an array of power electronic switching devices, that, with their fast switching action, can shape DC voltage to AC and AC to DC. While doing it, the phase and magnitude of AC voltage can be controlled, so as the power flow through the converter. While doing conversion, the harmonics are introduced into the power system also. The output square waveform is shown in Fig. 14 a). It consist of fundamental component and spectra of odd harmonics. In three phase configuration, due to 120^{o} phase shift between three output AC voltages third harmonic and its multiple will get canceled for balanced circuit in line to line voltage.

The advantage of the STATCOM over traditional synchronous compensator is lack of inertia providing fast response without introduction of oscillation and lack of rotational parts lowering maintenance requirements. The disadvantage is introduction of harmonics, rating of switching devises and switching losses and high initial cost. To decrease

harmonic content in the output voltage waveform, PWM or some other fast switching strategies has to be used but that may lead to increase in switching losses. Moreover, power switching devices has limited voltage and current ratings, so the switches have to be put in series and in parallel which may lead to gating problems.

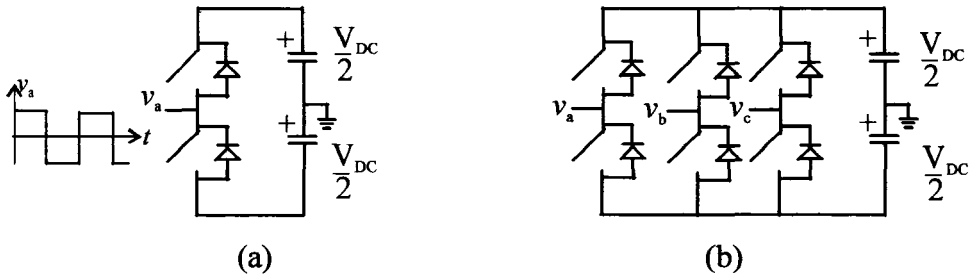


Figure 14 Basic six pulse converter circuit. a) one converter leg with its output AC voltage waveform, b) three phase circuit.

To decrease switching losses, increase rating and improve output voltage waveform, the six pulses converters are combined as shown in Fig.15, cascaded or multilevel topologies are used for power system applications.

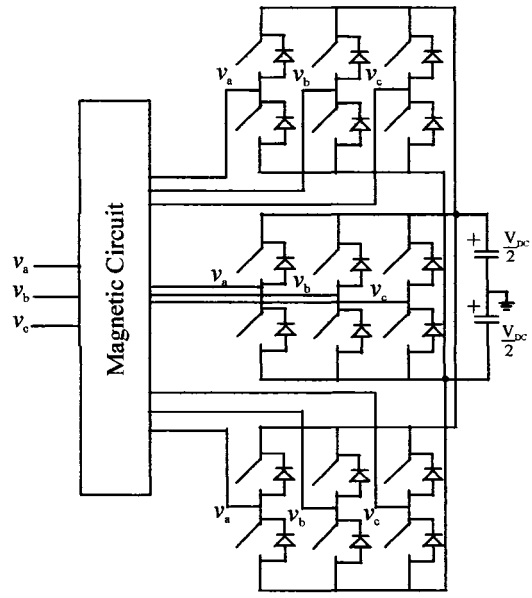


Figure 15 Inverter coupling with magnetic circuit

3.3 Diode Clamped VSC

One of the most popular multilevel converter topologies for high voltage application is so called "diode clamped" topology. Fig.16 shows one phase of five-level diode clamped VSI together with its output voltage waveform. The topology that was proposed by Nabae et al. [30] had initially only three levels controlled by PWM modulation strategy. The three-level diode clamped VSI gained a lot of attention for high voltage applications and, very soon, has been upgraded with the new levels [31] and enhanced [32]. Because of its advantages such as decreased THD, off-line optimization of switching angles, increased voltage rating and diminished dv/dt stress, the topology has been suggested for different high voltage applications such as STATCOM, UPFC and back to back DC link [35-38]. However, there are some important drawbacks such as complicated construction, unequal current stress on switching devices and capacitor voltage balancing problem. The capacitor voltage unbalance depends upon switching angles and net active power transferred between AC and DC side of inverter. If this transfer is zero, than the problem disappears. Because of the capacitor balancing problem, the most suitable application for diode clamped multilevel VSI is STATCOM. In the case of ideal STATCOM, the net active power exchange between AC and DC side of inverter circuit is zero during steady state operation. The capacitor balancing problem has been solved in [60].

3.3.1 Topology description

Fig.16 shows one phase of five-level diode clamped inverter. The DC bus of the N level inverter consists of N-1 capacitors that allow N taps for N levels of voltage. The capacitors are common for all three phases. One phase of power circuit has (N-1)x2 power switches and (N-2)x2 clamping diodes. Each switching devices has to stand one voltage level.

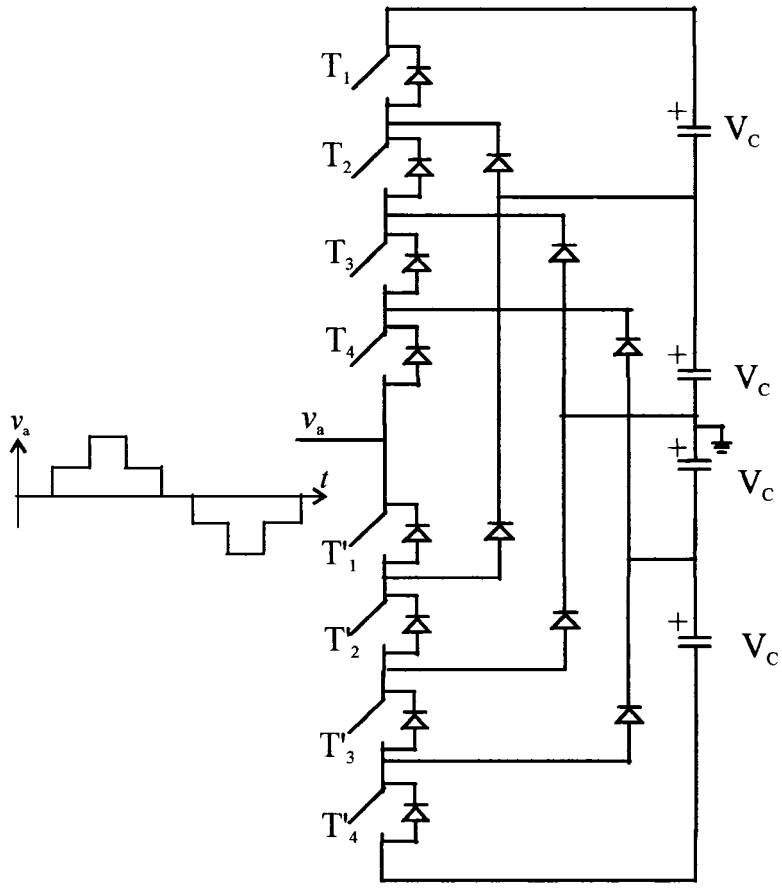


Figure 16 One leg of five level diode clamped voltage source converter

3.3.2 FFM Switching Strategy and Switching Functions

The FFM switching strategy is conceived on a premise that each switch commutes only twice over one cycle of fundamental frequency (once on and once off). This strategy of modulation may be difficult to accept in the case of six pulses inverter because of large amount of pollution in output voltage waveform. But in the case of multilevel inverter, if the number of level is sufficiently high, the distortion present in output voltage is small enough. Moreover, FFM is crucial for high voltage application because it allows a considerable decrease in switching losses. Fig.17 shows switching functions that allow generation of five-level staircase output voltage.

Switching devices T_1, T_2, T_3 and T_4 have for their complements T_1', T_2', T_3' and T_4'. If T_1 is forced to close, T_1' is forced to open and vice versa. The same is true for the other devices. The voltage on the DC side of the converter V_{DC} consists of four equal voltages V_C, where V_C is voltage across one of the four capacitors that form DC bus. The switching devices are controlled by switching function given by Fig 17. The shaded areas show that transistors are in conduction. Output voltage waveform consists of five-level $2V_C$, V_C, 0, $-V_C$ and $-2V_C$.

- to obtain voltage level $2V_C$, transistors T_1, T_2, T_3 and T_4 are closed and their complements T_1', T_2', T_3' and T_4' are open.
- to commute to voltage level V_C, transistor T_1 is forced to open an T_1' to close
- to commute to voltage level 0, T_2 is forced to open an T_2' to close.
- to commute to voltage level $-V_C$, T_3 is forced to open and T_3' to close
- to commute to voltage level $-2V_C$, T_4 is forced to open and T_4' to close.

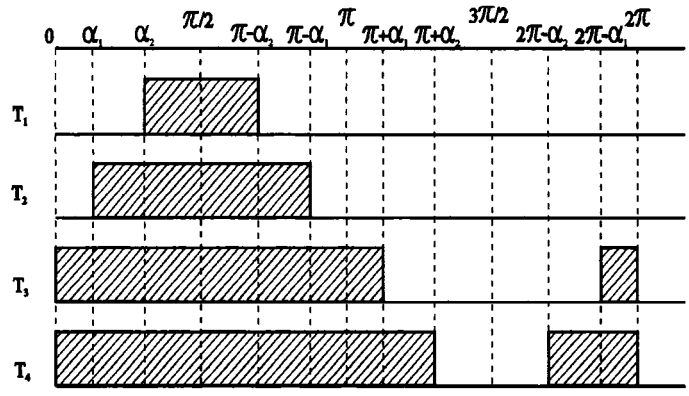


Figure 17 Switching function for five-level voltage source converter

By returning in reverse direction the full cycle is described. Repeating given pattern, the staircase quasi-sinusoidal voltage output waveform is obtained. The voltage stress on transistors dv/dt is limited to one level that is voltage V_C across one of the capacitor on the DC side of converter. The current path through converter depends on the voltage level and sign of the current. The current stress is not equally distributed among switching

devices and that it is more pronounced for inner switching devices (T_4 and T_1') than for outer switching devices (T_1 and T_4'). As a consequence, the rate of charging and discharging inner capacitors C_2 and C_3 is higher than that of outer capacitors C_1 and C_4, so that the voltage across the inner capacitors will tend to increase or decrease more than the voltage across outer capacitors, depending on the mode of operation (capacitive or inductive). The voltages across capacitors must be balanced in order to prevent distortion of the output voltage and to ensure the even voltage stress dv/dt in the switching devices. Equalizing DC capacitors voltages can be achieved by additional hardware [31] or within control algorithm [38],[60]. The voltage balance problem does not exist in case of ideal reactive operation (converter currant lead or lag converter voltage by 90 degrees).

3.3.3 Voltage Output Waveform: Optimization

In general, one N-level diode clamped VSI can produce N-level output voltage waveform (Fig.18) and the line-to-line voltage can consist of 2N-1 levels. If the FFM switching strategy is applied, then each switching device commutes twice per cycle, diminishing switching losses.

N-level output voltage waveform produced using FFM switching strategy (Fig.18) is symmetric and can be represented by series of Fourier:

$$v(t) = \sum_{k=1}^{\infty} \frac{4V_C}{\pi k} \left[\cos k\alpha_1 + \cos k\alpha_2 + \ldots + \cos k\alpha_{\frac{N-1}{2}} \right] \sin k\omega t \tag{3.1}$$

$$k = 2n+1, \quad n \in N$$

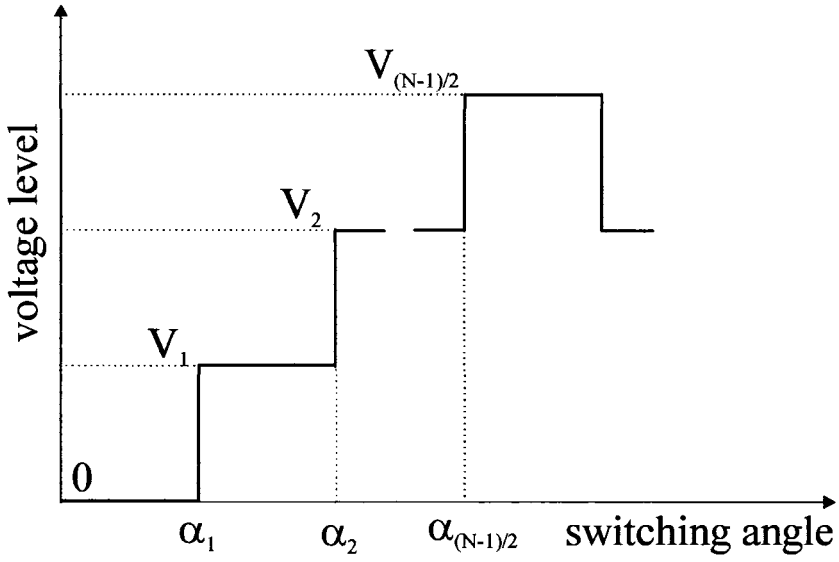


Figure 18 N-level output voltage waveform

From Fig. 18 it can be seen that for N-level output voltage waveform (N-1)/2 switching angles α_1, α_2 to $\alpha_{(N-1)/2}$ can be chosen in order to eliminate (N-1)/2 dominant harmonics or to minimize (total harmonic distortion) THD. In other words, N-level converter has (N-1)/2 degrees of liberty. The amplitude of k^{th} harmonic is given by (3.2).

$$A_k = \frac{4V_C}{\pi k}\left[\cos k\alpha_1 + \cos k\alpha_2 + \ldots + \cos k\alpha_{\frac{N-1}{2}}\right] \tag{3.2}$$

In the five-level output voltage waveform, two dominant harmonics can be eliminated (5^{th} and 7^{th}) by solving a set of equations given by (3.3), where A_i are Fourier coefficients given by (3.2) for i=5,7.

$$\begin{aligned} A_5 &= 0 \\ A_7 &= 0 \end{aligned} \tag{3.3}$$

After finding solutions from (3.3), THD of phase voltage is 21.7%. The third harmonic and its multiples are eliminated in the line-to-line voltage. The line-to-line voltage is given by (3.4) and THD of line-to-line voltage is 8.56%.

$$V_{line} = \sum_{k=1}^{\infty} A_k \left[\sin(k\omega t) - \sin k\left(\omega t - \frac{2\pi}{3} \right) \right] \tag{3.4}$$

The other solution, appropriate for one phase converter, is to minimize THD. The function of THD for the five-level inverter is given by (3.5) where $f(\alpha_1, \alpha_2)$ is given by (3.6).

$$THD\% = 100\sqrt{\frac{V_{RMS}^2}{V_1^2} - 1} = 100\sqrt{f(\alpha_1, \alpha_2) - 1} \tag{3.5}$$

$$f(\alpha_1, \alpha_2) = \frac{\pi}{4} \frac{\left(2\pi - \alpha_1 - 3\alpha_2\right)}{\left(\cos\alpha_1 + \cos\alpha_2\right)^2} \tag{3.6}$$

After minimizing the function $f(\alpha_1, \alpha_2)$, THD of the phase voltage is 16% and THD of line voltage is 10.8%. In both case the line voltage consists of nine levels. The RMS value of phase N-level output voltage is given by (3.7) and RMS of fundamental is given by (3.8).

$$V_{RMS}^2 = \frac{2V_C^2}{\pi} \left[\left(\frac{N-1}{2} \right)^2 \frac{\pi}{2} - \alpha_1 - 3\alpha_2 - 5\alpha_3 - 7\alpha_4 + \ldots + (N-2)\alpha_{\frac{N-1}{2}} \right] \tag{3.7}$$

$$V_{1RMS}^2 = \frac{8V_C^2}{\pi^2} \left[\cos\alpha_1 + \cos\alpha_2 + \ldots + \cos\alpha_{\frac{N-1}{2}} \right]^2 \tag{3.8}$$

It is worth noting that magnitude of the inverter output voltage, if the off-line optimization applied, depends exclusively on the value of the voltage V_C across the capacitor on the DC side of inverter. If the off-line optimization is not applied, then this magnitude can be controlled by changing switching angles α_i .More details an be found in [61]. Some other modulation strategies such as pulse width modulation (PWM) or selective harmonics elimination (SHEM), which result with even better output voltage waveform, can be used, but they impose higher speed of switching, which may not be acceptable in high voltage applications.

3.4 VSC Equivalent Circuit

Fig.19 illustrates three phase Voltage Source Converter equivalent circuit. The AC side of the converter is modeled by voltage sources v_a, v_b and v_c while DC side of the converter is modeled as current source I_{DC} and capacitance [46]. The DC current I_{DC} is converter DC current. To model the switching and capacitive losses the resistance can be added in DC side of the converter. The AC and DC side of the converter are related through power balance equation:

$$P = V_{DC} I_{DC} = v_a i_a + v_b i_b + v_c i_c \tag{3.9}$$

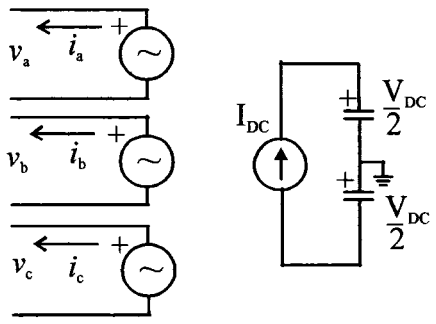


Figure 19 VSC equivalent circuit

3.5 Proposed Control Strategy for STATCOM

Fig.20 shows block diagram of the STATCOM control circuit. The primary objective of the control system is to provide the adequate voltage support. This is achieved by controlling the amplitude of STATCOM output voltage as described in section 2.6. When voltage support is needed, the STATCOM output voltage is increased, and STATCOM provides reactive power. During period of light loading of transmission line, when voltage has tendency to arise, the STATCOM output voltage decreases, STATCOM absorbs reactive power (or supply less reactive power), and controls the line voltages as illustrated on vector diagrams in Fig. 7 a) and b). A detailed description of control strategy is given in [62,63]. In this work the control strategy is conceived on low frequency PWM modulation. The DC voltage on DC bus of the power converter is kept constant. The relation between amplitude of STATCOM output voltage $V_{STAT.}$, and the voltage on the DC bus V_{DC} is given by:

$$V_{STAT.} = m\frac{V_{DC}}{2} \tag{3.10}$$

where m is modulation index. In order to control $V_{STAT.}$, the modulation index m is varied and DC bus voltage is kept constant. The outer control loop allows active power control. The PLL (phase lock loop) allows synchronization of the STATCOM output voltage with the AC system. Its robustness is crucial for the performance of the STATCOM. The PLL must be able to lock up the phase of line voltage immediately after disturbances. Its output is phase angle. DC bus voltage of the STATCOM is measured, filtered and compared to the reference value. The error is processed through Proportional-Integral (PI) block. The output of PI block is used as phase shift reference δ that is added to PLL output. The sum of the two signals gives phase angle reference for the STATCOM output voltage allowing the flow of active power from line into the STATCOM in order to meet its losses. The inner control loop has faster dynamic and allows reactive power control.

The instantaneous values of the three phase voltages v_a, v_b and v_c on the supported bus are measured and RMS value of midpoint voltage V_{RMS}. is computed using

$$V_{RMS} = \sqrt{\frac{1}{3}(v_a^2 + v_b^2 + v_c^2)} \tag{3.11}$$

The computed value is compared with V^*_{RMS} the desired value of the line voltage. The error signal is processed in PI block and applied as modulation index. The distinct advantages of this type of control are following:

1. There is no need to measure current, therefore, getting rid of the current transformers.
2. The active and reactive power control are completely decoupled.

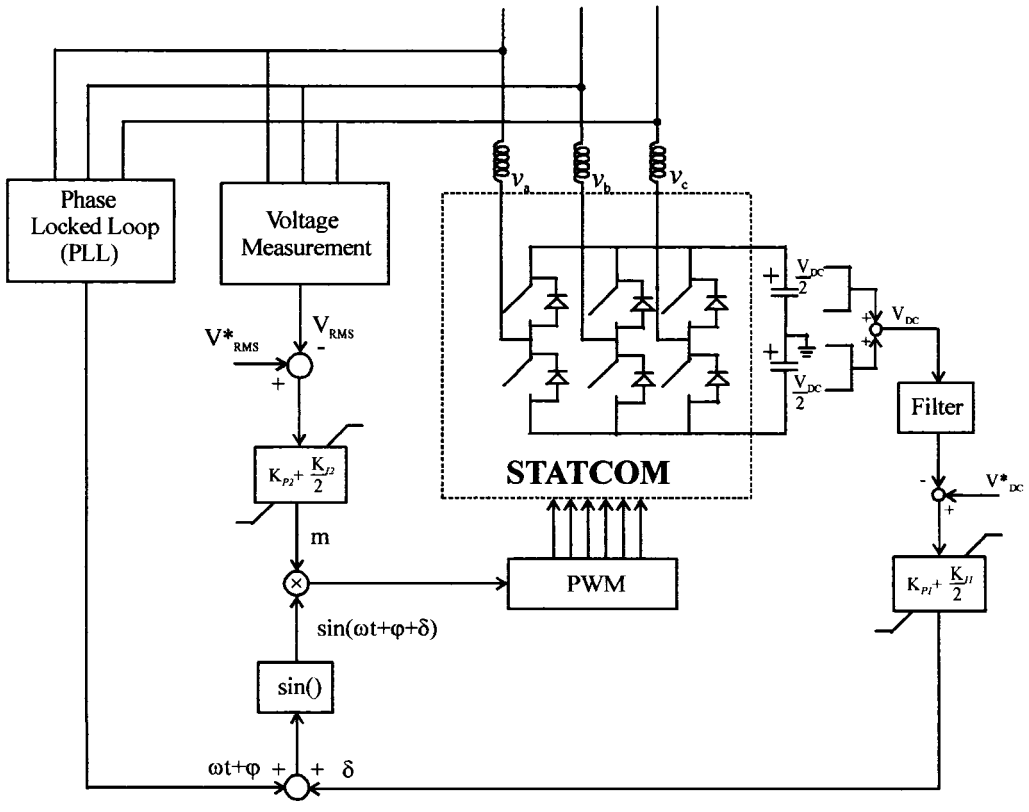


Figure 20 STATCOM control circuit

3.5.1 Phased lock loop (PLL)

Fig. 21 shows the structure of PLL. The PLL is designed for three phase operation.

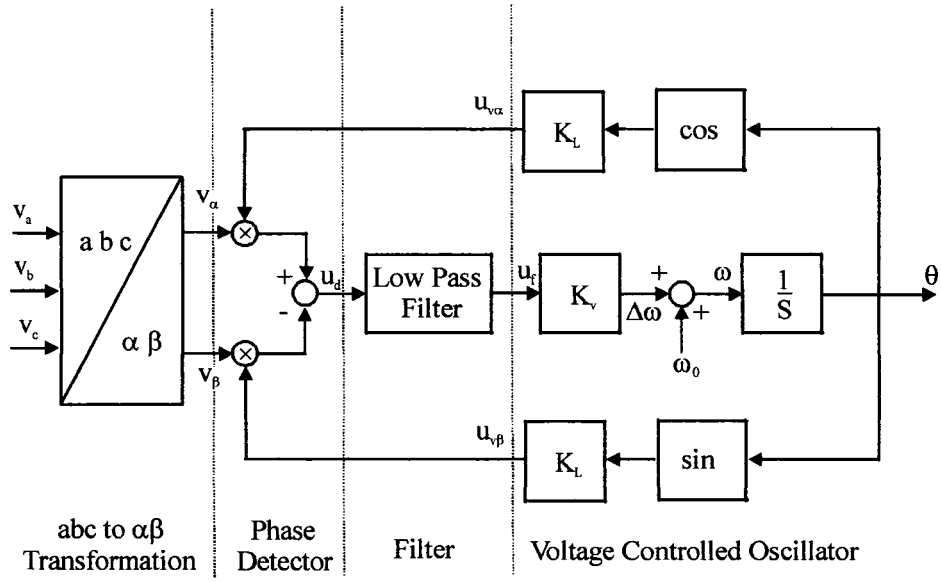


Figure 21 Phased lock loop-block diagram

The instantaneous line voltages v_a, v_b and v_c are measured and transformed in α–β reference frame. The PLL consist of three parts: phase detector, filter and voltage controlled oscillator. The line voltages are given by:

$$\begin{aligned} v_a &= V_{max.} \sin(\omega t + \varphi) \\ v_b &= V_{max.} \sin(\omega t + \varphi - \frac{2\pi}{3}) \\ v_c &= V_{max.} \sin(\omega t + \varphi + \frac{2\pi}{3}) \end{aligned} \tag{3.12}$$

After the transformation in in α–β reference (3.12) becomes (3.13).

$$v_\alpha = V_{\max.} \sin(\omega t + \varphi)$$
$$v_\beta = V_{\max.} \cos(\omega t + \varphi) \tag{3.13}$$

The phase angle of the line voltage is ωt+φ. The output of the phase detector is given by (3.14):

$$u_d = v_\alpha u_{v\alpha} - v_\beta u_{v\beta} = V_{\max} K_L \left[\sin(\omega t + \varphi)\cos\theta - \cos(\omega t + \varphi)\sin\theta\right] = V_{\max} K_L \sin(\omega t + \varphi - \theta) \tag{3.14}$$

Angle θ can be written as $\theta = \omega t + \varphi_1$ therefore (3.14) becomes:

$$u_d = V_{\max} K_L \sin(\varphi - \varphi_1) \tag{3.15}$$

Assuming that PLL is locked, (3.15) can be linearized and rewritten as:

$$u_d = V_{\max} K_L (\varphi - \varphi_1) \tag{3.16}$$

Signal obtained from (3.15) is passed through low pass filter that is PI block whose proportional and integral gains are K_P and K_I respectively so the output of the filter is:

$$U_f(S) = V_{\max} K_L (\varphi - \varphi_1)\left(K_P + \frac{K_I}{S}\right) \tag{3.17}$$

$\Delta\omega = K_V u_f$

$\omega = \omega_0 + \Delta\omega$

where ω is PLL frequency and finally phase angle is:

$$\theta = \omega_0 t + \int_{-\infty}^{t} \Delta\omega dt \tag{3.18}$$

3.5.2 Positioning of STATCOM

The optimal positioning of voltage support devices in transmission line has been investigated in [9,63],[65-67]. It has been stated in [9,65] that, when dynamic voltage support devices positioned in mid point of the transmission line power transfer can be doubled. The voltage profile of the line is given with solution of the wave equation:

$$\frac{d^2V}{dx^2} = \left[(r + j\omega l)(g + j\omega c)\right]V \tag{3.19}$$

Assuming lossless line the solution is given by:

$$\bar{V} = \bar{V}_R \cos\beta x + jZ_c\bar{I}_R \sin\beta x \tag{3.20}$$

Z_C is characteristic impedance of the line

$\beta = \omega\sqrt{lc}$ is wave number

l-line inductance (H/km)

c-line capacitance (F/km)

If the active and reactive power of the load are P+jQ, the sending end voltage(source voltage) is (3.21):

$$V_S = V_R \cos\theta + jZ_C \frac{P - jQ}{V_R} \sin\theta \tag{3.21}$$

V_R receiving end voltage

V_S sending end voltage

$\theta=\beta l$, l line length (km),

θ - electrical line length

The voltage $\mathbf{V_R}$ can be taken as reference, $\mathbf{V_S}$ can be written as (3.22)

$$\mathbf{V_S} = |\mathbf{V_S}|(\cos\delta + j\sin\delta) \qquad (3.22)$$
$$\mathbf{V_R} = |\mathbf{V_R}|$$

Combining (3.21) and (3.22) yield (3.23)

$$V_S \sin\delta = Z_C \frac{P}{V_R} \sin\theta \qquad (3.23)$$

From (3.23) the power transfer between two ends of the line is given by (3.24)

$$P_R = \frac{V_S V_R}{Z_C \sin\theta} \sin\delta \qquad (3.24)$$

where V_S is sending end voltage, θ is the electrical length of the line ($\theta=\beta l$) and δ is power angle. From (3.24) it is obvious that maximum power transfer occurs when δ is 90 degrees. If we assume that $|V_R| = |V_S| = |V|$, then steady state stability limit is (3.25).

$$P_{MAX.} = \frac{|V|^2}{Z_C \sin\theta} \qquad (3.25)$$

If the line voltage is supported by mid point sitting voltage source then the line can be considered to be made of the two section each having electrical length $\theta/2$. In this case (3.24) becomes:

$$P_R = \frac{V_S V_M}{Z_C \sin\frac{\theta}{2}} \sin\frac{\delta}{2} \tag{3.26}$$

where $| V_M | = |V|$ is mid-point voltage.

In this case the steady state stability limit is given by (3.27)

$$P_{MAX.COMP} = \frac{|V|^2}{Z_C \sin\frac{\theta}{2}} \tag{3.27}$$

The increment in steady state maximum power transfer depends upon the line length and is expressed as (3.28):

$$P_{MAX.COMP} = P_{MAX.} \frac{\sin\theta}{\sin\frac{\theta}{2}} \tag{3.28}$$

where $P_{MAX.COMP.}$ is maximum steady state transferable power of mid-point compensated line and $P_{MAX.}$ is maximum steady state transferable power of the non-compensated same line. In case of short line $\sin\theta \sim \theta$ and $\sin(\theta/2) \sim \theta/2$ and (3.28) becomes (3.29)

$$P_{MAX.COMP} = 2P_{MAX.} \tag{3.29}$$

In the reality, the maximum power that can be transferred over the transmission line is limited by transient stability of the power system. The transient stability limit can be determined by using equal-area stability criterion. The stable operation of mid point compensated line with controllable voltage source is extended in the second quadrant ($90^0 < \delta < 180^0$).

3.6 Simulation Studies

The objectives of the simulation are to evaluate dynamic response of the proposed control strategy and to evaluate how much one can increase power transfer over existing, long transmission line with mid point sitting of STATCOM for voltage support, using detailed models of all components. The simulated network consists of a 400 km long radial 735 kV transmission line. The line is energized by 10,000 MVA hydro-turbine. The simulation parameters are given in Appendix A. Other end of the line is attached to infinite bus so that we have a classical, one machine system, swinging around infinite bus. The STATCOM is positioned in the midpoint of the transmission line as illustrated in Fig.22.

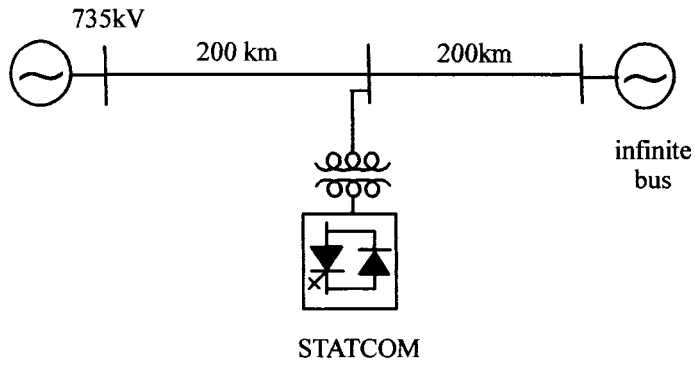


Figure 22 Single line diagram of the test network

3.6.1 STATCOM Dynamic Response

Figures 23 and 24 show STATCOM dynamic response for 10% step change of reference signals. Fig.23 (upper trace) shows system response for 10% step down and 10% step up (lower trace) change of reference voltage V_{RMS}. At the same time, Fig.23 illustrates STATCOM regulation capabilities. Fig.24 a) and b) shows STATCOM response for 10% step up and 10% step down change on DC reference V_{DC}.

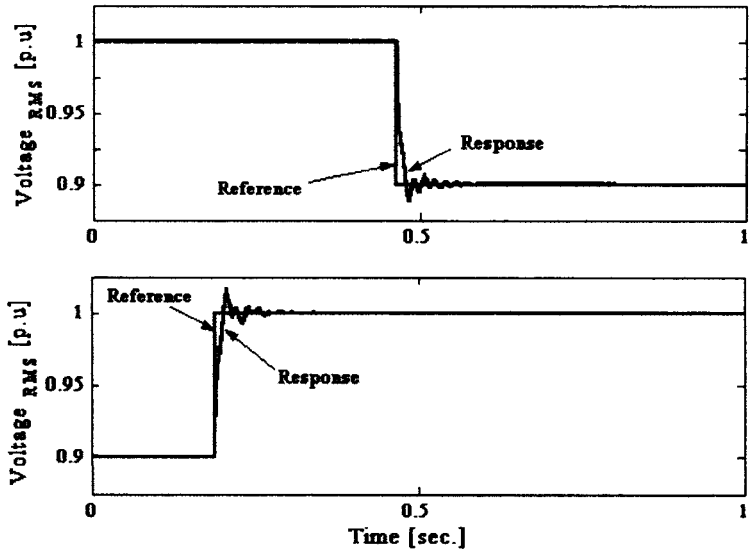
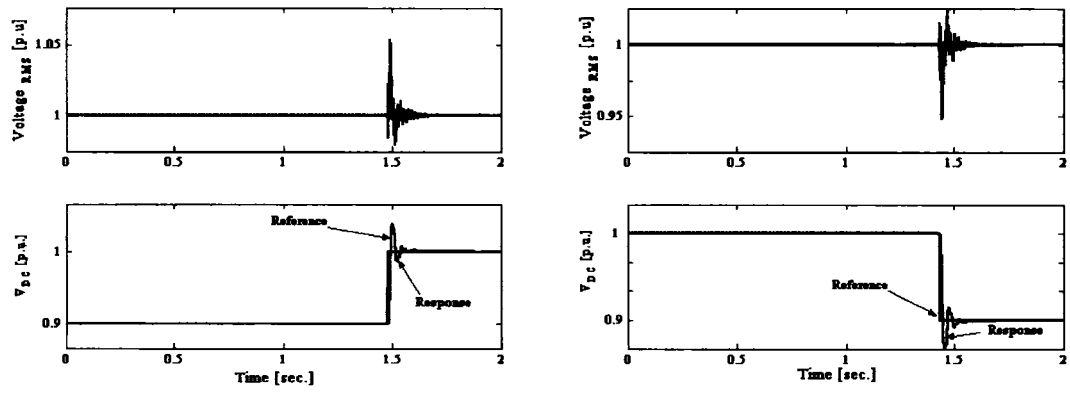


Figure 23 STATCOM dynamic response for 10% step down change in reference voltage and 10% step up change in reference voltage



(a) (b)

Figure 24 a) STATCOM dynamic response for 10 % step up change in DC reference. Upper trace shows measured AC line voltage and lower trace shows DC bus voltage. b) STATCOM dynamic response for 10 % step down change in DC reference.

3.6.2 Steady State Stability

In order to investigate the power transfer steady state and transient stability limits, the system described above is simulated without and with STATCOM. For the analysis of steady-state performance, the power supplied by the generator-turbine unit is increased gradually. After each power increment, the simulated system is allowed to regain the stable point of operation. The power transferred over the line is measured. The maximum power that can be stably transferred without mid-point sitting STATCOM for voltage support is 4300 MW. When the STATCOM installed, the maximum power increases to 7450 MW. One can see that power transfer is increased during the steady-state by the factor of 1.732. The power transfer is not increased by the factor of two as expected in [65]. The reason is while power is increased, the line and transformer losses increase because of higher current. The second reason is that the line voltage is already naturally supported by line distributed shunt capacitance as shown in (3.28).

3.6.3 Transient Stability

The same system is subjected to transient stability test. The power loading is increased gradually and system is allowed to stabilize. Then three phase short circuit is applied in the vicinity of the generator unit (30 km from generator) and is cleared after 100 ms. The system must reestablish to the same power transfer level as before the short circuit in order to remain stable. The maximum power that can be transferred stably is 4000 MW without the STATCOM and 6400 MW with STATCOM sat in the middle of the line, which is an increase by a factor of 1.6.

3.7 Conclusion

The STATCOM based on power converter has been discussed in this chapter. An original control strategy for voltage support of transmission lines by STATCOM has been

presented and evaluated using a test system. The results of case analysis obtained by detailed numerical simulation have shown that STATCOM can significantly increase steady state and transient stability limits and hence transmission capacity of existing lines, while providing voltage support. When STATCOM put in the middle of the 400 km, 735 kV line, it is known to be optimal placing for the radial line, the steady state stability limit is increased by 73% and transient stability limit is increased by 60%. The power transfer can not be doubled due to the line length, losses and transformer and generator impedances. At the same time, voltage of the line is kept constant, independently of the loading which contributes significantly to power quality. It makes STATCOM attractive and cost effective alternative to building new line.