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LIST OF ABREVIATIONS AND ACRONYMS

ADC	Analog to Digital Conversion
CM	Common Mode
DM	Differential Mode
DSC	Digital Signal Controller
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
FEM	Finite Element Method
GIR	General Impedance Representation
IA	Impedance Analyzer
LISN	Line Impedance Stabilization Network
LDO	Low Dropout Linear Regulator
PCB	Printed Circuit Board
PEEC	Partial Element Equivalent Circuit
PSRR	Power Supply Rejection Ratio
PWM	Pulse Width Modulation
OP-AMP	Operational Amplifier
NIF	Node - to - node Impedance Function
NR	Newton - Raphson
THD	Total Distortion Harmonic

VNA	Vector Network Analyzer
VTG	Voltage Transfer Gain

LISTE OF SYMBOLS AND UNITS OF MEASUREMENTS

A	Current unit Ampere
F	Capacitor unit Farad
H	Inductor unit Henry
V	Voltage unit Volt
Ω	Resistor unit Ohm
Hz	Frequency unit Hertz
dB	Logarithmic unit Decibel
W	Active power unit Watt
μ	Micro or 10^{-6}
m	Milli or 10^{-3}
k	Kilo or 10^{3}
M	Mega or 10^{6}

INTRODUCTION

Noise in power converter is an important topic which has been extensively researched. Typically, there are two types of noise mentioned in power converter researches:

- Electromagnetic Interference (EMI): noise generated by the converter, propagating to the grid, which impacts other circuits or device's operation. To limit these effects, EMI of each power converter must be controlled under certain levels given by standards such as FCC, CISPR11, CISPR22, IEC61000-4, MIL-STD-461, etc;
- Noise immunity: the noise picked up by the converter from the other circuits or devices in the grid, affecting the converter's performance. The converter must be designed to prevent this noise to degrade its performance.

Both types of related to the interactions between the power converter and other devices. On the other hand, there is another kind of noise inside the power converter, which can degrade the performance of control circuits. It is the noise in the low power circuit of the power converter. This noise results from the switching transients of power transistors. This noise type is not well addressed in literature, hence, it remains a difficult topic with multiple relating sub-topics for research. In order to fulfill this lack in literature, the problematic of this type noise will be introduced in the next sections of this chapter and the sub-research topics will be presented in the remaining chapters of this thesis.

Origin of Noise in Low Power Circuit

The first question arises is that "How is noise in low power circuit is generated by the switching transients of power transistor?". The answer of this question is the high frequency current created during turn - off intervals of the power transistor, it is explained below by the switching transient analysis.

When voltage applied on the Gate of power transistor is higher than the its Gate threshold voltage ($V_{GS} > V_{GS(th)}$), the transistor is at ON state with $V_{DS} = 0$. The current flows from $+VDC$ to the load, as given in Fig. 0.1.

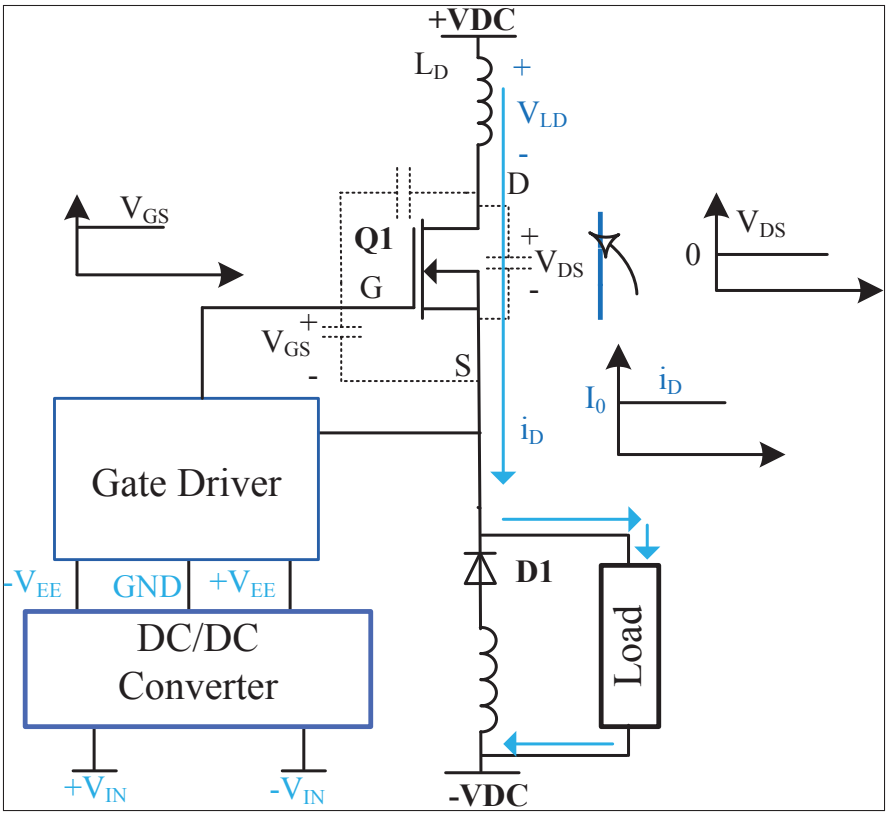


Figure 0.1 Current paths during ON state of power transistor

When voltage applied on the Gate of power transistor is lower than its Gate threshold voltage ($V_{GS} < V_{GS(th)}$), the transistor is turning to OFF state. At this moment, the voltage across DS junction, V_{DS}, increases. Consequently, voltage on stray inductance between Drain and $+VDC$, V_{LD}, changes creating current flowing to Miller capacitance, C_{GD}, of the power transistor. This current is a significant part of the noise current, i_G, in the Gate driver. This current propagates to the low power circuit via the isolation capacitance of the DC/DC converter supplying the gate driver. This process is shown in Fig. 0.2. The effect of i_{GD} on the noise spectrum in low power circuit will be presented by experimental results in Chapter 2.

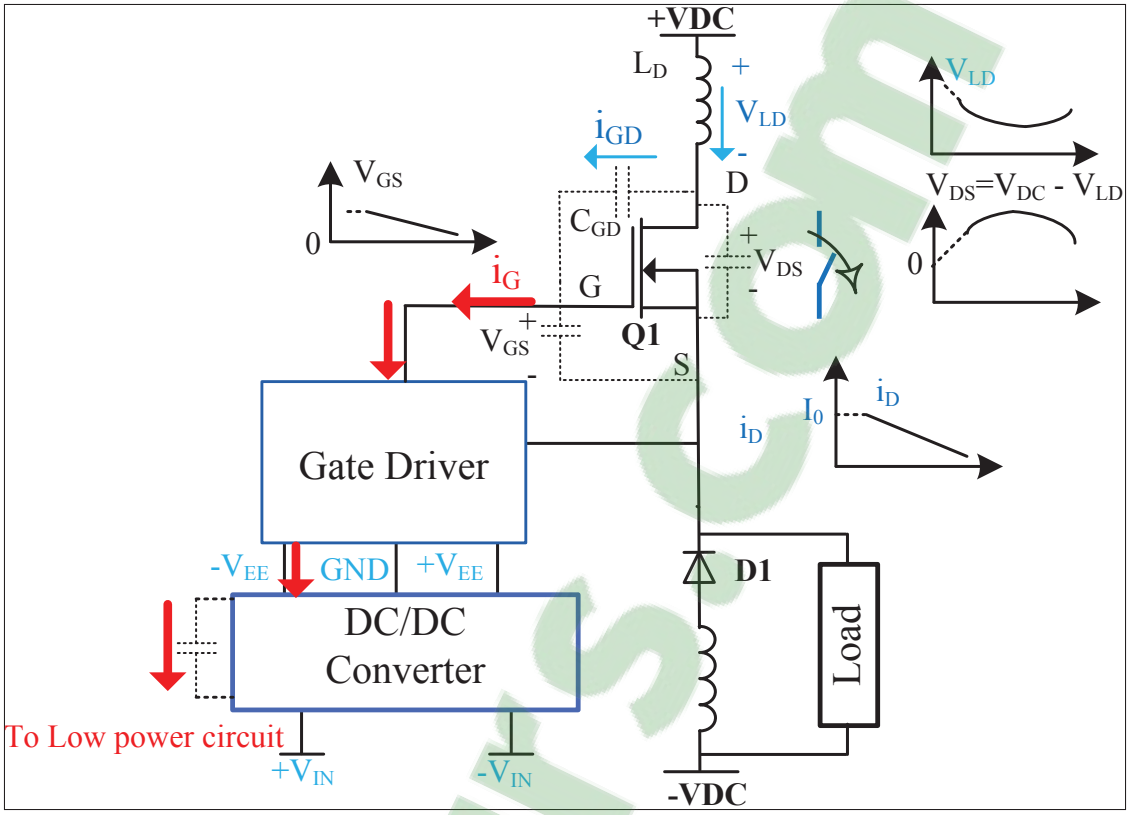


Figure 0.2 Noise current generated during turn - off intervals of power transistor

Research Problematic

As pointed before, noise is generated by the switching transients of the power transistors of the high power circuit and propagates to the low power circuit through parasitic capacitive barriers. The definitions of high and low power circuits are presented in Fig. 0.3, which shows a typical power converter structure. The high power circuit includes the components operating on high voltage and current levels such as power transistors, DC bus filter, input filter, current and voltage sensors. The low power circuit contains the components operating on low voltage and current such as sensing circuit, i.e. outputs of voltage/current sensors with their amplifiers, DSP/micro-controller, gate driver to control the high power transistors, and power supplies of these functional circuits.

The detailed view of the low power circuit of a typical power converter is illustrated in Fig. 0.4. In this structure, an isolated DC/DC converter (PS1) regulates a $+12V$ voltage from the power

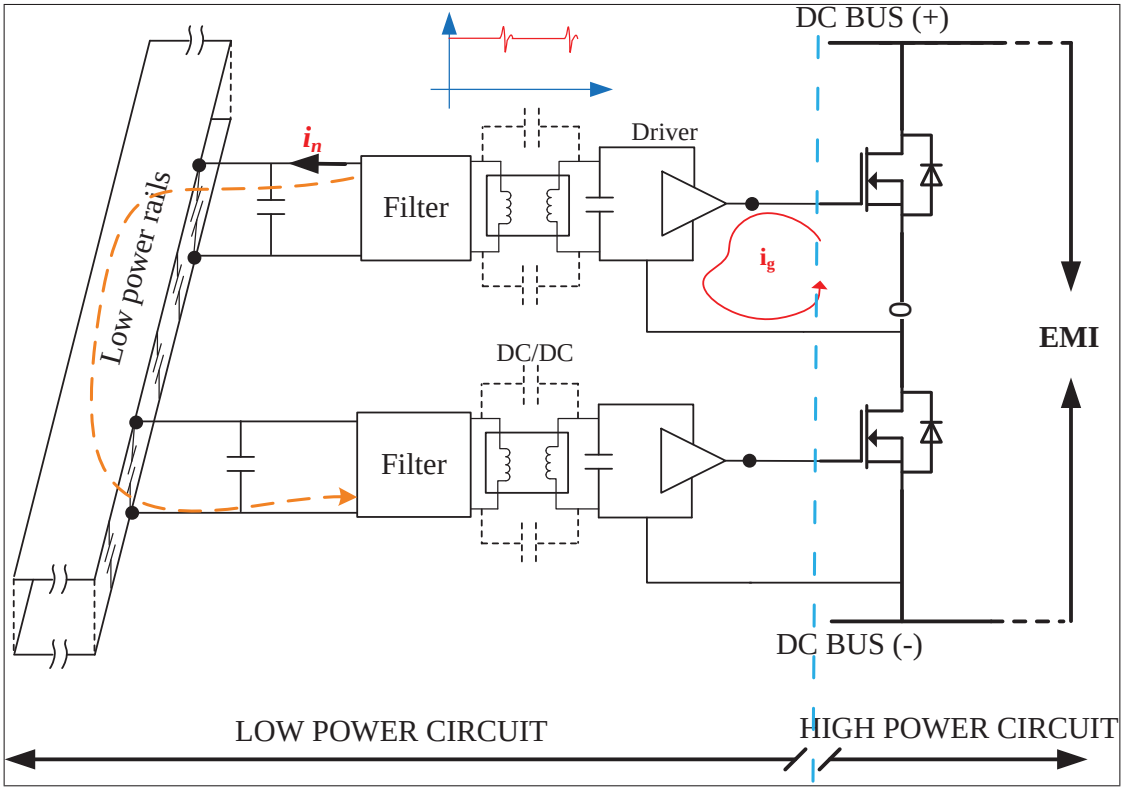


Figure 0.3 Power converter structure including high power and low power circuit

source. The output of this DC/DC converter is connected to a low voltage power rails distributing power for the other DC/DC converters. These isolated DC/DC converters (PS2, PS3, PS4) provide positive and negative rails to supply gate drivers and micro-controllers. During the converter power operation, the switching process of them generates very high $\partial V/\partial t$ across power transistors, propagating noise through the numerous stray capacitances in the converter structure. This noise travels along the connecting traces, passes through parasitic elements of gate drivers and distributed DC/DC converters before reaching the low power rails, where low power control circuits are located.

The parasitic capacitance between the input and output sides of the DC/DC converters (PS2, PS3, PS4), defined as isolated capacitance in manufacturer's documentations, is usually low, i.e. in the range of hundreds of pF. However, its combination with the surrounding impedance, i.e. the low power rails and impedances of functional circuits, can provide an easy way for noise to propagate in EMI frequency range. Once in the low power rails, the noise propa-

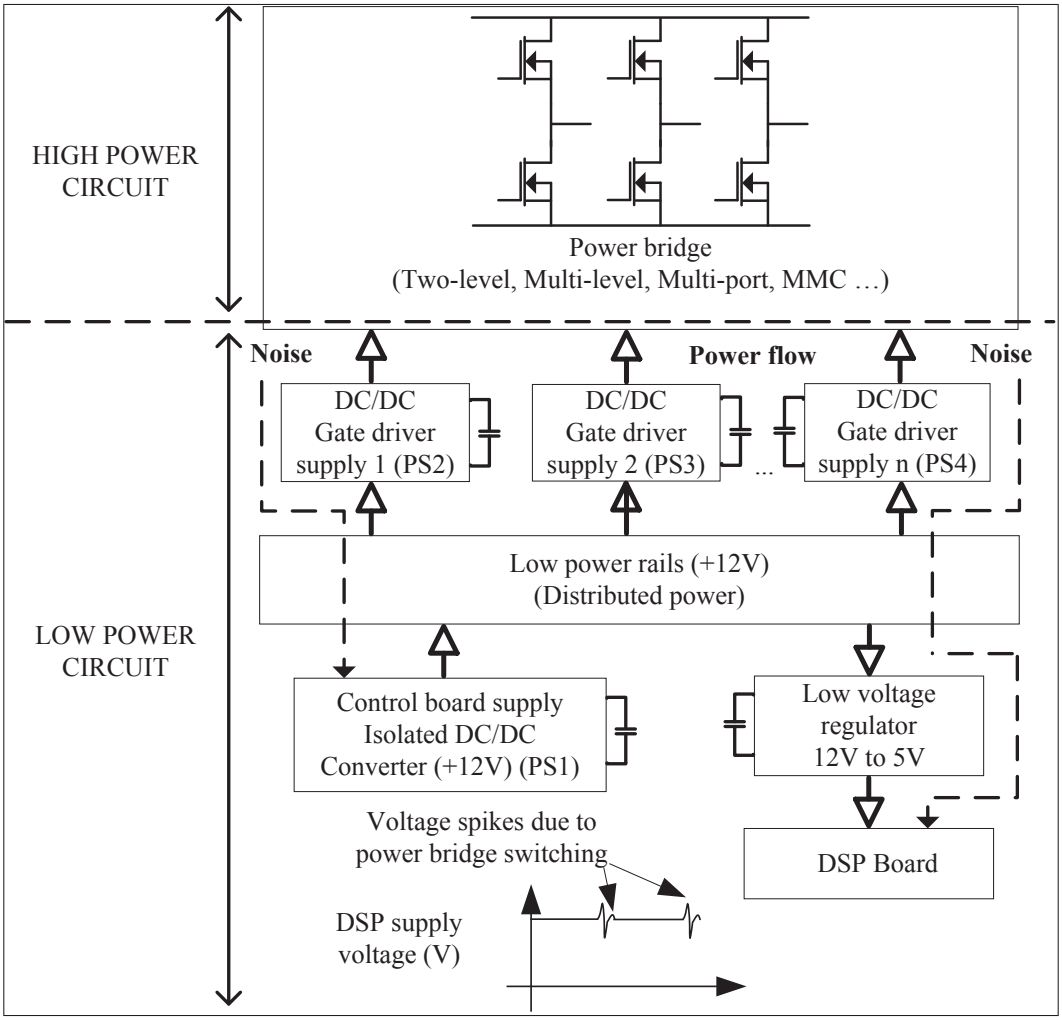


Figure 0.4 Noise propagation in low power circuit of converter

gates in a complex way to other DC/DC converters and other low-voltage devices, resulting in voltage spikes in their supply. These voltage spikes can cause inaccurate voltage and current measurements, malfunction of DSP and gate drivers, altering the overall reliability of the power converter. To avoid this issue and ensure the converter reliability, noise in the low power circuit must be handled carefully in the early design state.

Example of Impact of Noise in Low Power Circuit

As mentioned previously, noise in low power circuit degrades the converter reliability, but how bad can its impact be? This section aims to provide an example of a typical gate signals

controller of an H-bridge, as shown in Fig. 0.5. In order to prevent the current shoot-through where both transistors Q_1 and Q_2 are ON at the same moment, a dead-time is added between their triggering signals. This task is performed by the dead-time generator circuit. Input of the dead-time generator circuit is the comparison output of the control and carrier signals. In this scheme, the carrier signal (ramp) is generated by an Op-AMP based circuit. Due to very low power supply rejection ratio (PSRR) of the Op-AMP in EMI frequency range, it is expected that noise in its power supply will present on the output signal. An experiment is conducted to check the effect of noise on Op-AMP power supply to the performance of overall circuit.

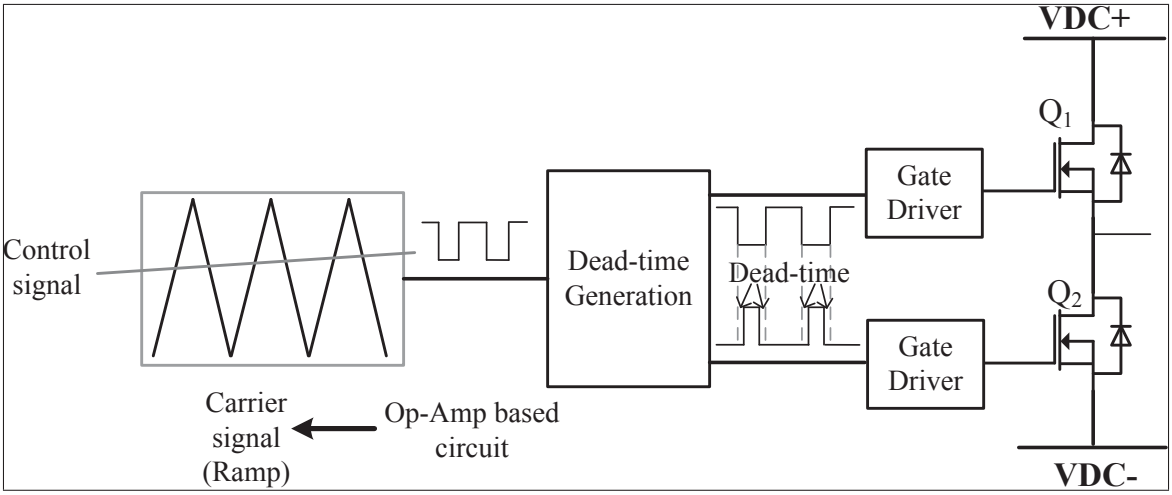


Figure 0.5 Dead-time generator scheme for an H-bridge

In good ground integrity condition, there is no noise on the Ramp signal while the gate signals are clean, and the dead-time is controlled at 200*ns*, as shown in Fig. 0.6.

In case of bad ground integrity, where ground of the Ramp generator circuit is connected to that of the control board by small wire, high frequency noise appears on the Ramp signal, as illustrated in Fig. 0.7. Consequently, the dead-time generator circuit input has multiple commutations. Therefore, the dead-time is wrong. For instance, there are 350*ns* and 0*ns* dead-time periods instead of the designed period of 200*ns*. Once high frequency noise increases, the overlap period of 50*ns* between 2 gate signals appears creating current shoot-through in the DC bus, which can damage the power converter.

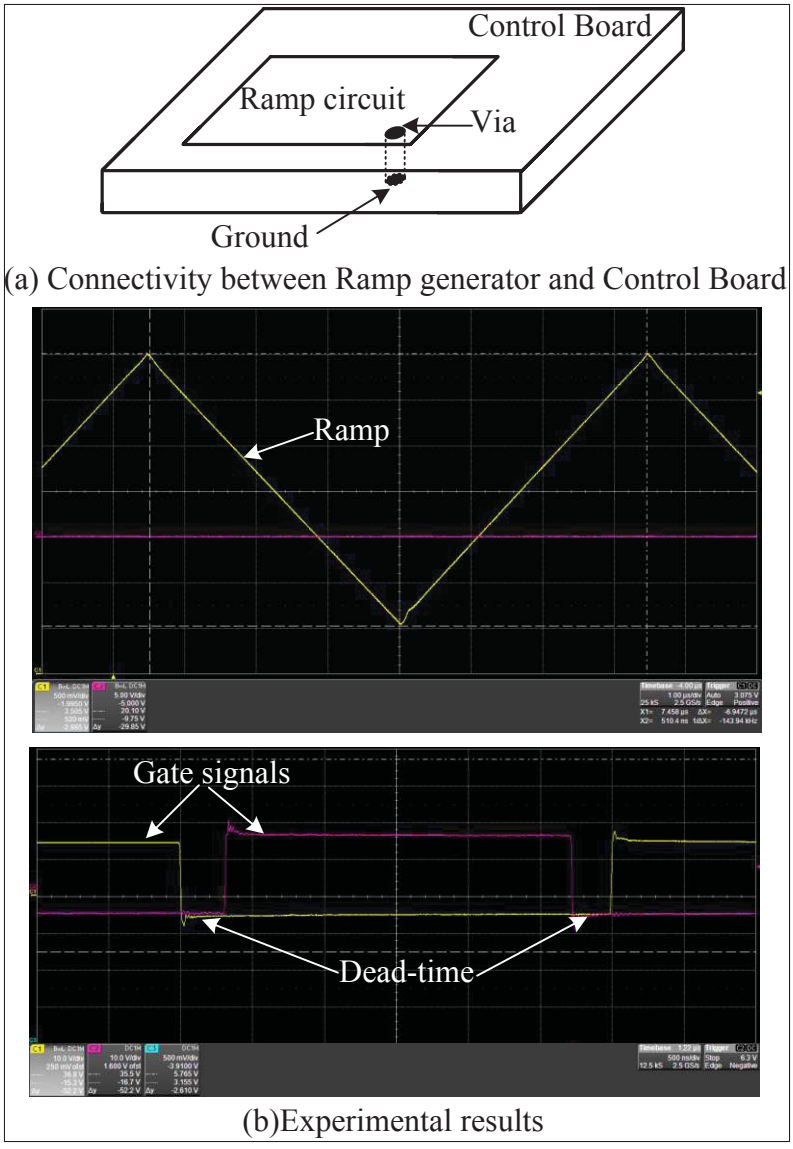


Figure 0.6 Performance of gate signals with good ground integrity

Motivation and Challenges

Power converter reliability is always a critical concern for industrial applications. Amongst the factors degrading power converter reliability, noise in low power circuit is an important issue as pointed previously. Meanwhile, it is difficult for the designers to handle this issue due to following reasons:

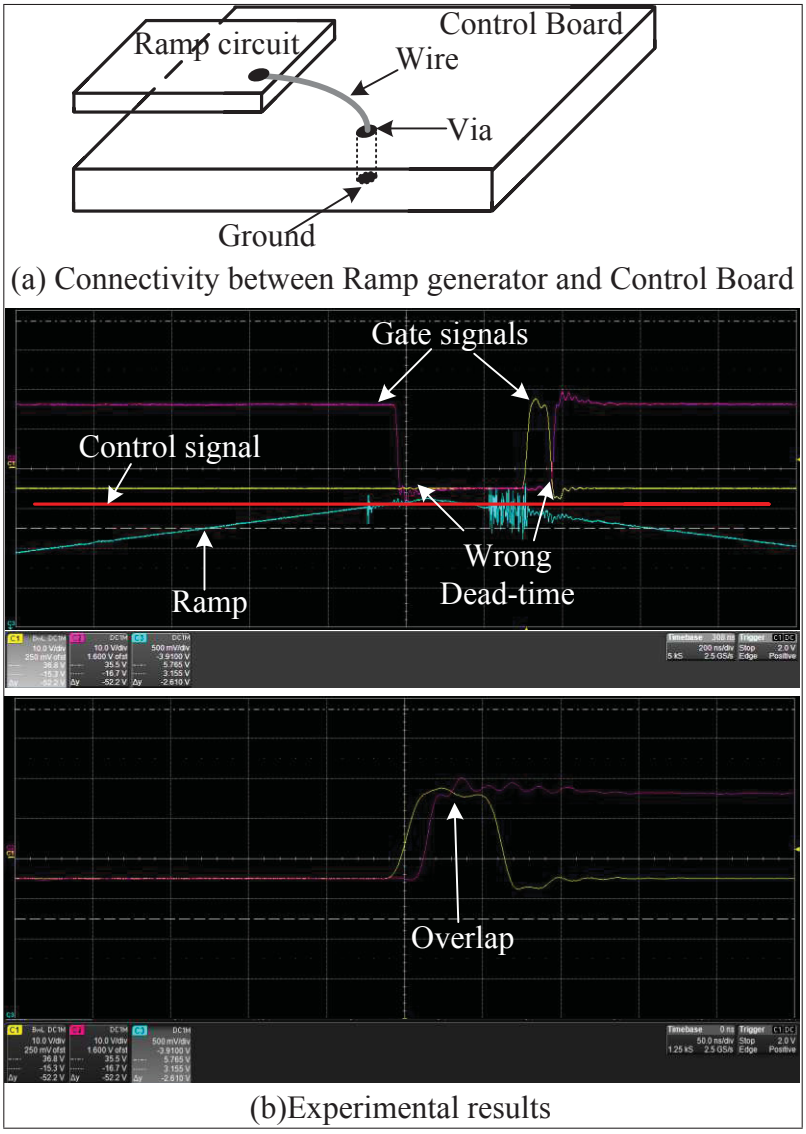


Figure 0.7 Performance of gate signals with bad ground integrity

First, noise in low power circuit does not have direct impact on the power converter performance. Instead, noise can create errors at an input of a control circuit (feedback signals) or on the controller supply. Hence, the controller reacts to these errors providing wrong control signals. On the other hand, noise can be added directly to the control signals in its propagation paths. In both cases, errors on control signals easily lead to bad converter performance such as degraded total distortion harmonic (THD) and pulse width modulation (PWM) jittering.

Second, noise may not be constant over time and may not be repeatable since it depends on transistor switching dynamic which changes with converter operating points. For example, duty cycle and switching frequency of power transistors change with different load demands and topologies (such as modern flyback). In addition, noise attenuation performance of filters changes with current/voltage bias conditions. These facts make noise difficult to observe.

Third, noise measurement in low power circuit during power converter operation is a tricky task. In fact, noise obtained in measurements is affected by the additional impedance of the measurement devices (such as voltage probe). Moreover, the common mode noise will increase with the additional paths provided by multiple measurement probes. These altered measured results mislead the debugging process. More dangerously, in case of improper measurement setup, the additional paths given by the measurement probes can create circulating current between the converter and the measurement devices, giving wrong converter operation or even damage both the converter and the measurement devices.

Due to the aforementioned reasons, noise mitigation in power converter is a difficult task. Specifically, this issue becomes more critical with such recent developments of power converters. First, SiC and GaN devices with short rising and falling times create noise in higher frequency than Si - devices (Kim *et al.*, 2017; Rondon-Pinilla *et al.*, 2014; Basu & Undeland, 2013; Han *et al.*, 2017a). In high frequency range (over 30MHz), noise mitigation is more difficult due to degraded filtering performance of the components. Second, control circuits become more complex in multi-level and multi-port converters with more devices and large dimensions of the common low power rails. In this case, noise is more difficult to manage due to complicated interactions between impedance of the low power rails and impedance of numerous components supplied by this rail.

Until now, there is no complete research for noise mitigation in low power circuit. Majority of power converter design guidelines for typical circuits were issued from know-how and practical experiences without computational models. On the other hand, the high frequency propagation problems, which can be applied for such case of noise, have been studied by the microwave

researches without direct application to power converters. Recently, the computational - based modeling techniques for noise prediction in power converter such as FEM and PEEC have been developed. However, taking into consideration the complete converter doesn't give the designers the ability to improve noise profile by changing design of typical components. Therefore, it is mandatory to develop a guideline for complete power converter design procedure based on computational models and insights of component effect on noise profile. It will help designers to understand well noise issue in converter resulting in improved design of each component to achieve low noise profile converter. The research presented in this thesis is performed to reach this goal.

In order to achieve the research targets, several challenges must be overcome in addition to the lack of references in literature and simulation tools.

First, it is necessary to observe noise and its influence on converter performance and reliability. Then, it is essential to divide the complex problem of noise propagation in a large low power circuit into smaller research objectives, and focus on small specific targets.

Second, since the research is performed based on measurement, the measurement setup must be selected correctly to avoid wrong measurement results. Taken into account the significant contribution of small inductive (in the range of nH) and capacitive elements (in the range of nF) on the total impedance in EMI frequency range, it is difficult to perform correct impedance measurements even with a modern device such Vector Network Analyzer (VNA). Every detail in the experimental setup must be taken care of to avoid errors in results.

Last but not least, the proposed modeling techniques must be validated in different components and different parameters to ensure its accuracy in general cases. The components and parameters for validation must be chosen properly and errors during measurement must be considered.

Research Objectives and Contributions

As mentioned before, this thesis focuses on several small specific research objectives in order to understand and improve noise profile in the low power circuit. The research contributions are listed as below.

1. In chapter 2, introduce noise issue in low power circuit and propagation paths inside the power converter, which are not well - addressed in literature;
2. In Chapters 3 and 4, propose new impedance models for the fundamental parts of the low power circuit such as passive devices and low power rails;
3. In Chapter 5, analyze and suggest an attenuation method for high frequency noise at the gate driver.
4. In Chapter 6, suggest a complete design process to achieve a low noise profile - low power circuit.

Methodology

The research of all chapters in this thesis is performed by the following steps:

1. Literature review: The literature relating to the research objects are reviewed from basic to state - of - the - art to understand the problem itself and figure out their limit on the application of the research topic to improve;
2. Experimental observations: Since the topic of noise in low power circuit has not been well-addressed in literature, experimental observations are important to identify the research objectives. Variety of measurements have been performed with setups for each objective to define whether change in each part leads to change in noise profile;
3. Mathematical model development: Based on experimental observations and the literature review, mathematical models are developed;

4. Experimental verifications: The proposed mathematical models are validated with experimental measurements for different design to confirm its accuracy. If errors appear with the measurement results, the mathematical model will be further improved.

Conclusion

In this chapter, we have introduced the problematic of the research presented in this thesis. The research on noise propagation in low power circuit is important to ensure power converter's high performance and reliability. Despite of its importance, it is still a big lack in literature for several reasons. The research presented in this thesis will contribute to to fulfill a part of this gap. In addition, we also presented the objectives, challenges and methodology to conduct the research.

CHAPTER 1

LITERATURE REVIEW OF NOISE ISSUES IN POWER CONVERTER

Noise propagation in the low power circuit is an important factor which impacts performance and reliability of power converters, as pointed in the previous chapter. A complete research on this area should consist of defining noise sources, analyzing propagation paths and developing noise mitigation techniques. Inspite of a deep litterature review, this topic has not been well covered in literature. However, separated parts of the project are studied in different relating research areas, as shown in Fig. 1.1.

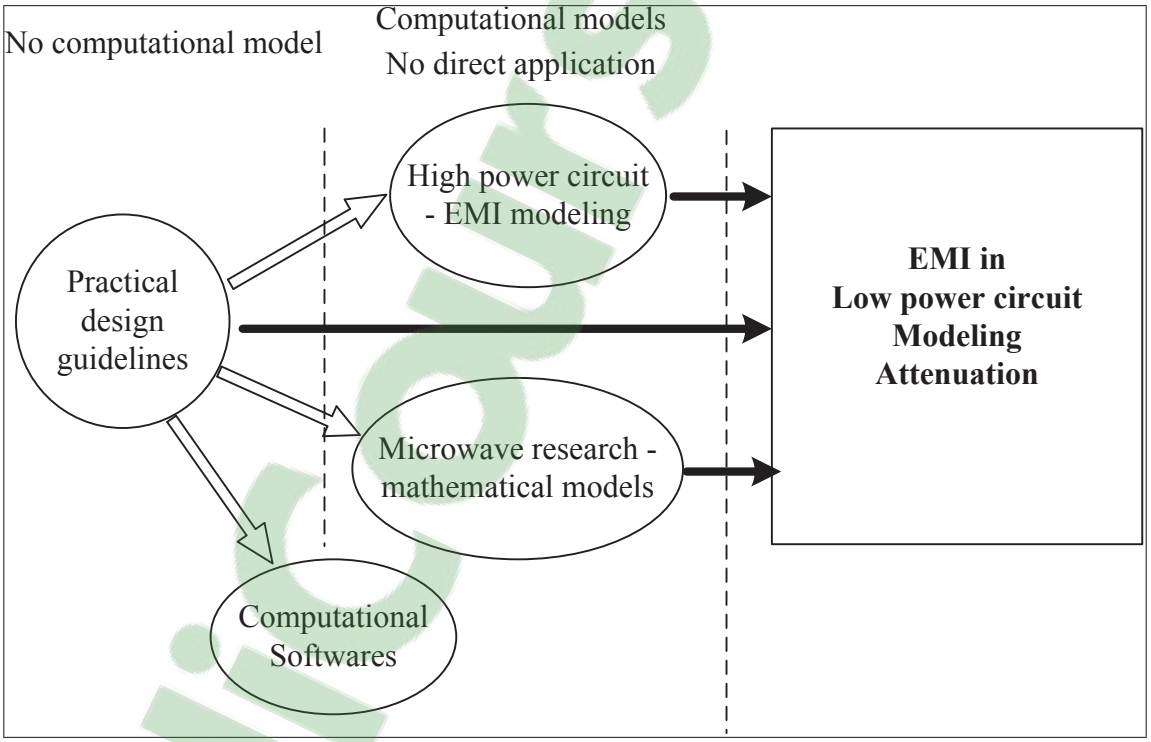


Figure 1.1 Research topic and state - of - the - art literature

First, since converter design is indeed practical, we can start with the practical design guidelines summarized by the experience designers and component manufacturers. However, the *know - how* is not proven by mathematical models. This fact can lead to improper design in specific cases requiring more design iterations with high cost and time consuming. Thus,

the computational model for each part of the circuit is mandatory to guarantee good design in term of noise minimization. This is the general motivation of the research presented in this thesis. We not only follow the fundamental design guidelines as practical designers, but we also research on the mathematical models of the circuit. It helps to understand for which cases guidelines are applicable or not and further improve them. As general speaking, we try to improve the practical guidelines by providing their bases of theories and computation. The computational models, as introduced previously as research objectives, can be researched by applying knowledge of relevant topics as below.

- Noise source analysis, filter design and mitigation techniques can be studied based on knowledge in the area of EMI modeling of high power circuit;
- PCB structure models can be referred to area of microwave researches which are conducted for high frequency applications;
- Some specific PCB structure models can be extracted by computational softwares.

Even though the outcomes of these studies are very useful, they are not directly applicable to our main research topic due to different objectives and applications. Since these topics are identical, it is more convenient to present their comprehensive reviews in the relevant chapters. In the next sections of this chapter, we will summarize the literature at high level to provide the overall view of related research areas, how they are useful to our research and what are the limits making them not directly employed to the main research topic.

1.1 Practical design guidelines

The know - how to design low noise power converter is represented by the practical design guidelines. These guidelines are introduced in design handbooks (Johnson *et al.*, 1993; Salman & Friedman, 2012; Horowitz & Hill, 1989) and manufacturer's documentations (TI, 2001, 2015). These guidelines provide excellent practice for high speed signal integrity such

as: routing laws for gate driver, supply and ground planes in mixed - signal PCB, use of decoupling capacitors and ferrite beads, and so on. However, these suggestions are not based on mathematical model, so it is difficult to employ in specific cases. Below are some examples:

1. Ferrite beads are suggested to prevent high frequency noise arriving at the *victim circuit* in high frequency. The ferrite bead impedance is the sum of its resistive and inductive parts. In case that the *victim circuit* has capacitive impedance, the total impedance of ferrite bead and *victim circuit* is represented by the resistive part at the resonant frequency created by the capacitive and inductive parts (serial LCR circuit). So, which ferrite bead impedance curve should be used to avoid noise amplification in a certain frequency range? Where will noise propagate if it is blocked from the *victim circuit*?;

2. In order to supply a circuit, a low power rails with power/ground plane structure is used to connect that circuit and the source. It is to minimize the impedance between these two circuits, preventing voltage spikes on the target circuit. EMI attenuators such as decoupling capacitors and filters are used to further attenuate noise. Usually, the decoupling capacitors are distributed along the low power rails and the filters are connected directly to the circuits. However, how to distribute decoupling capacitors on the low power rails? Which value of the capacitors should be used for a specific converter structure (different power transistors and layout of low power circuit lead to different noise frequencies, and hence, different values and locations of decoupling capacitors)? Which filters should be used? How impedance of the filter interact with that of the low power rails? Can it ensure noise attenuation or result in noise amplification in certain frequency ranges? These issues become more complex in case that numerous circuits are placed on the low power rails.

In such above cases, one must use a *trial - error* approach in several design iterations until an acceptable noise level is achieved. However, these above questions can be answered in early design phase by using computational tools to analyze the circuit and ensure a reliable design. There are mathematical models in research areas discussed in the following sections.

1.2 Research of EMI in high power circuit

EMI in high power circuit of power converter has been the essential research topic over the last ten years. Several efforts have been made to obtain EMI prediction for a whole power converter (Espina *et al.*, 2011; Rondon-Pinilla *et al.*, 2014; Ferber *et al.*, 2013; Zhai *et al.*, 2015; Ardon *et al.*, 2010; Musznicki *et al.*, 2013; Mrad *et al.*, 2013). In addition, in order to meet conducted EMI standards, passive and active EMI filters are used to attenuate noise. They have been improved in terms of frequency response (Raggl *et al.*, 2010; Akagi & Shimizu, 2008; McDowell & Hubing, 2015; Shin *et al.*, 2015) and density (Biela *et al.*, 2009; Maillet *et al.*, 2010).

These researches provide the insights of noise origin, EMI analysis, and EMI filter. These knowledge are the proper basics for conducting research on EMI in low power circuit. However, they are not always valid to employ directly in board level due to the following reasons.

1. On board level, CM and DM are not well - defined and separated as in high power circuit due to multiple propagation paths provided by PCB structures and components. Thus, CM and DM models of the filter developed for high power circuit are not valid in low power circuit;

2. In high power circuits, EMI model of a complete converter can be the summary of several parts whose impedance can be measured directly (Zhai *et al.*, 2015). This approach is valid since each part can be considered as a two - port circuit. However, at board level, the low power rails is a multi-port circuit. Hence, which impedance can be used to compute noise propagation while there are plenty of the port - to - port impedance? Since impedance is not effective to evaluate noise propagation, what can be used?;

3. In high power circuit, EMI attenuation is mostly focused on EMI filter design to comply with standards. Therefore, EMI filter is designed with the only purpose of preventing noise to propagate to the input of the converter. However, in low power circuit, the situation is more complicated. Since noise always propagate on the low impedance paths, increasing

impedance at one port by the filter can result in noise increasing at the other ports of the circuit. Therefore, “where should we block noise and where should we let noise propagate to?”. This is a challenge that designers must face. Such difficulties clearly show that care must not only be taken in the local design, but also the complete circuit.

1.3 Microwave researches

As pointed above, multi-port PCB structures are usually designed in low power circuit. In order to study noise propagation in low power circuit, analysis of these structure in high frequencies (up to hundreds of MHz) must be done. It is not focused in power electronics area, but has been a popular topic in microwave researchs (Pozar, 2009). Power/ground planes structure used for low power rails design is analyzed with either rectangular (Lei *et al.*, 1999; Hampe & Dickmann, 2005; Fan *et al.*, 2001) or arbitrary geometries (Štumpf & Leone, 2009; Štumpf, 2014; Smith *et al.*, 2001; Bednarz *et al.*, 2014; Lee *et al.*, 2015), including effects of decoupling capacitors (Kim *et al.*, 2004; Guo & Hubing, 2006; Hampe *et al.*, 2007; Kim & Swaminathan, 2001). The transmission line effect, skin effect and proximity effect are important to consider in these high frequencies (Haus & Melcher, 1989). In addition, the PCB structure without current returned path, which is popular in low power circuit, is developed by the powerful Partial Element Equivalent Circuit (PEEC) model.

However, these methods are not directly applicable to the low power circuit due to following reasons. First, since these models are developed for very high frequency applications (can be up to *GHz*), several effects are considered making the models complicated and not practical to employ for power electronic applications. Second, these models are not flexible to merge into a larger model with numerous other components used in the low power circuit. Therefore, more practical and flexible modeling approaches must be developed to predict noise in low power circuits.

1.4 Computational softwares

Beside mathematical approaches introduced previously, there are softwares that can be used to extract the parasitic elements of devices and PCB structures such as FastHenry, FastCap (free), Q3D Ansoft, StarRC, QRC (commercial). These softwares are developed based on mathematical methods such as Finite Element Method (FEM), PEEC and Method-of-Moment (MoM). Even though softwares provide many advantages, engineers must have knowledge of the problem's physics and valid conditions of the software for effective utilization. In addition, the available softwares are not able to compute the EMI model of a complete low power circuit including arbitrary PCB structures and numerous passive and active devices. Furthermore, since these softwares only provide the extracted result of completely built component or PCB structure, they do not provide information to improve the design for lower noise profile.

Due to these above limits, in our point of view, softwares can be used for PCB structures that require complex mathematical models such as thin power/ground plane or PCB trace without current return path underneath. However, they are not effective for modeling a complete circuit.

1.5 Conclusion

In this chapter, a general review of the topic of noise in low power circuit has been presented. As pointed before, due to the lack of literature on the main research topic, it is divided into small specific targets which are related to other research areas such as practical design guidelines, EMI in high power circuit and microwave research. This chapter also introduces the advantages and limits of these studies in term of application to EMI research in low power circuit. Based on these discussions, each specific objective will be developed using the basics of relevant research topics.

The research contributions will be presented in the next chapters of this thesis, as summarized in Fig. 1.2. Chapter 2 provides the experimental evidences of noise propagation inside power converter, which is the reason for conducting the research presented in this thesis. The proposed modeling approaches for passive devices (GIR) and low power rails are introduced in Chapters

3 and 4, respectively. Chapter 5 presents the Y-cap application method to attenuate noise at high frequency where EMI filter is not effective. The complete design process to minimize noise in low power circuit is suggested in Chapter 6. Finally, the conclusion and recommendations for future works are presented.

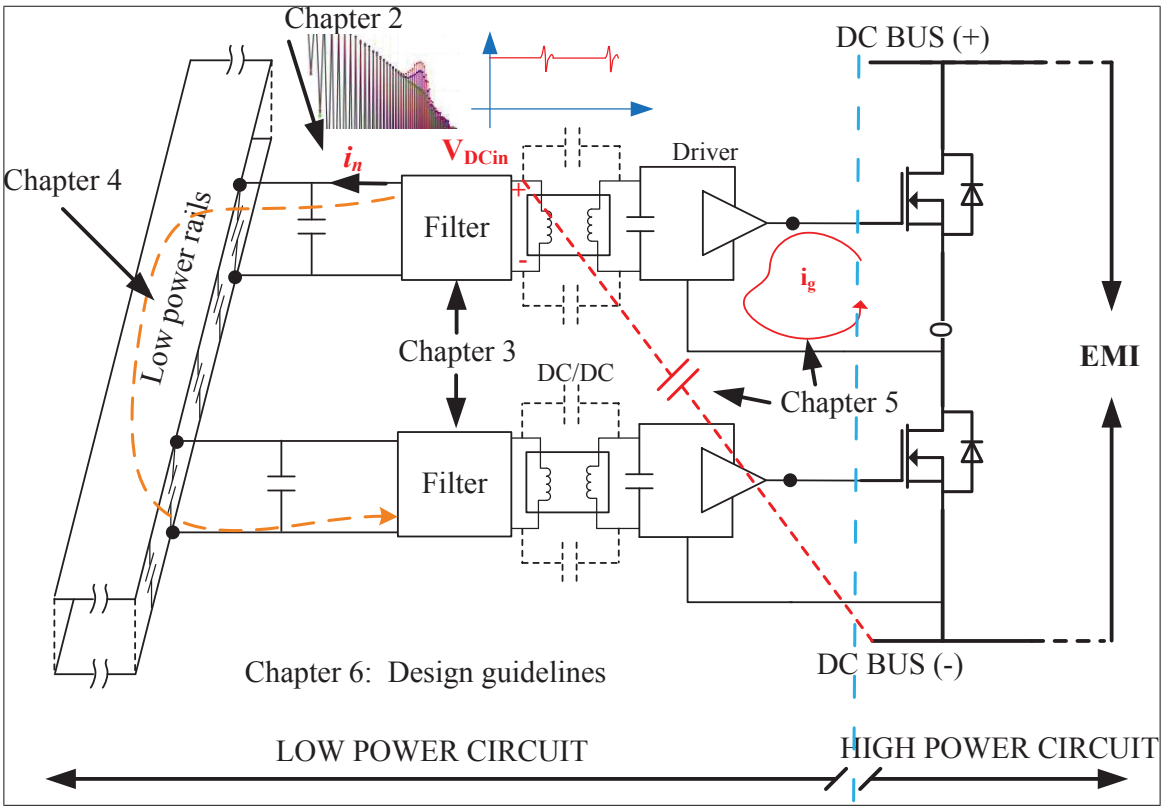


Figure 1.2 Graphical thesis outline

CHAPTER 2

EXPERIMENTAL INVESTIGATION OF NOISE PROPAGATION IN LOW POWER CIRCUIT OF POWER CONVERTER

Summary

As pointed before, there is a lack of literature on noise propagation in low power circuit, meaning that this topic has not been mentioned in research. Therefore, the first topic is to prove the existence of the problem itself. It is done by measuring noise and observing its changes with different designs and operating points of the power converter. This content is presented in this chapter by experiment results on a typical Buck converter designed for noise measurement purpose. This chapter also introduces the voltage variation limits of fundamental components to emphasize the importance of noise control in the low power circuit.

2.1 Introduction

While Silicon MOSFET has been used in power converter applications for decades, Silicon Carbine MOSFET (SiCMOS) has been developed in the last 10 years. Due to the high switching frequency of SiCMOS, the sizes of key components in the converter such as magnetic devices (input inductors of the Buck/Boost/Rectifier, transformers of the Flyback) and output capacitors can be reduced while the current and voltage ripples are maintained in the acceptable ranges (Biela *et al.*, 2011). Therefore, SiCMOS is the key to achieve high power density converter design. However, the sharp voltage applied on the SiCMOS during very high switching operation with short rise and fall times result in voltage ringing across the switching devices at very high frequency, i.e. 50 - 100MHz, due to the effect of stray inductance and device's parasitic capacitances (Han & Sarlioglu, 2016) - (Li & Munk-Nielsen, 2014). An example of the voltage ringing across Drain - Source (V_{DS}) of the SiCFET is shown in Fig. 2.1 which is captured from (Shi *et al.*, 2017). This voltage ring produces higher EMI than standard Si-based converters in the conducted EMI frequency range (10 - 30MHz) (Kim *et al.*, 2017; Rondon-Pinilla *et al.*, 2014; Basu & Undeland, 2013; Han *et al.*, 2017a). Moreover, the voltage and

current spectra through switching devices in SiC - based converters are 20-30dBμV and 20 - 30dBμA higher than those in the Si-based ones in frequency range from 20 to 100MHz, respectively (Oswald *et al.*, 2014). These augmented spectral contents at high frequency will be translated into significant increase of EMI at the converter input (Zare *et al.*, 2015).

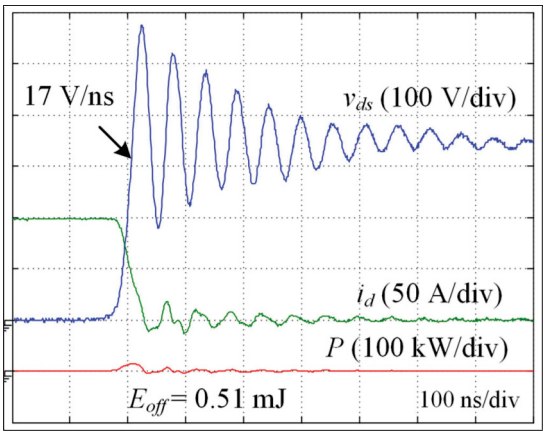


Figure 2.1 Turn - off switching waveform of SiC MOSFET module
Taken from Shi *et al.* (2017)

On the other hand, these voltage ringings can propagate to the Gate of power transistors, resulting in voltage oscillation on the Gate - Source (V_{GS}) during transient time (Clemente *et al.*, 1987; Nguyen & Blanchette, 2017). Taking into account the fact that small gate resistor is required to minimize the delay time on rising/falling edges and minimize the power dissipation during high frequency switching operation of the SiCFET, the high frequency voltage ringing appearing on V_{GS} can be seen by all the components in the Gate driver circuit, including the output of Gate driver power supply. From there, these voltage ringings can propagate to the input of the DC/DC converter, i.e. low power rail, by passing through its *parasitic capacitance* (Nguyen *et al.*, 2017c). The low power rail voltage waveform of a reduced scale Buck converter, which will be introduced in Chapter 5, is shown in Fig. 2.2 with a quite high voltage variation at high frequency, i.e. 200mV at 10MHz and 550mV at 60MHz.

From the low power rails, this noise can result in voltage spikes on the components. Although no standard exists on an acceptable noise margin, each component has strong requirements

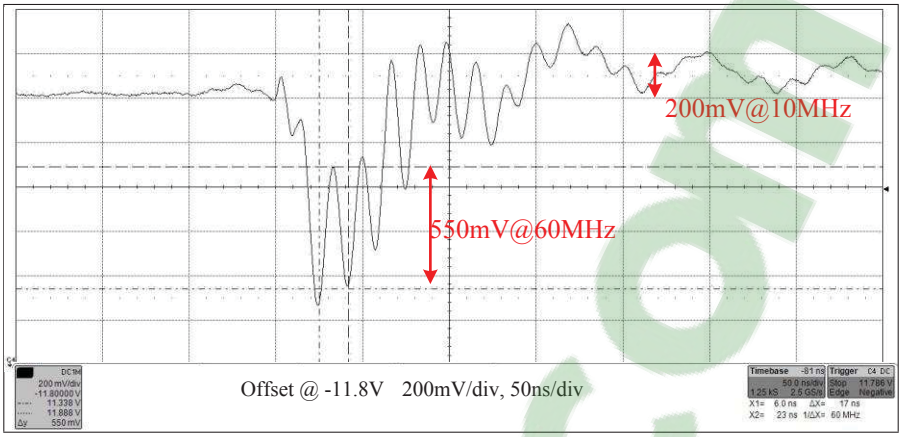


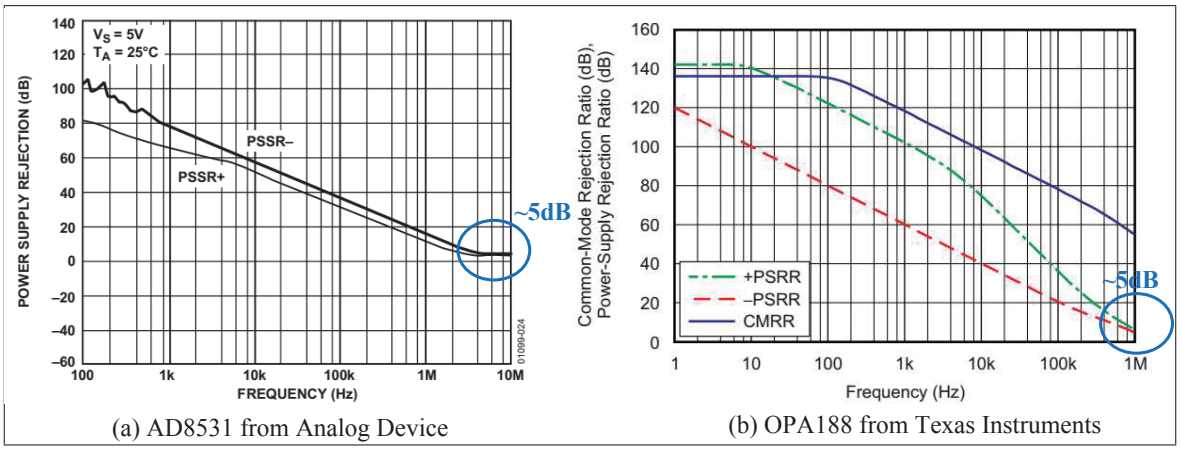
Figure 2.2 Voltage ringing at low power rail of a laboratory Buck converter

on their supply variation, which are usually described in the manufacturer's documentations. Below are the examples of characteristics related to noise on power supply of two important components in low power circuit such as the digital signal controller (DSC) and operational amplifier (Op-amp).

- In the DSC case, the limit of its power supply variation is $\pm 5\%$ (TI, 2016), which is equivalent to the limit of $165mV$ variation in absolute value. However, the noise margin required for proper operation is much more critical. As suggested by the manufacturer (TI, 2015), the power supply noise must be quite low to not influence the ADC's step size of $732\mu V$ for the input range of 0-3V. In addition, the reference voltage for ADC block must be less than $100\mu V$. Violating these limits will increase the on-chip PLL jittering which impacts the controller precision, which is mandatory to ensure low THD waveforms;

- The Op-amps are usually used in current and voltage sensing circuits. Their outputs are connected to the ADC inputs of the controller. Therefore, noise and errors on its outputs are critical to achieve accurate control. However, the Op-amp power supply rejection ratio (PSRR) is very low inside the EMI frequency range, meaning that noise appearing on its power supply can propagate into the outputs with few or no attenuation. For instance, as examples shown in Fig. 2.3a and b, the PSRR of the AD8531 and OPA188 is less than 5dB at frequency over 3MHz and 1MHz, respectively. Assuming that there is $200mV$ noise at

the power supply at 3MHz considering the single supply of 5VDC, the noise observed at the output is $150mV$, which is equivalent to 3% error of the full sensing range. Depending on the sampling rate of the controller, this error can randomly appear on the controller computation. Once all the sensed signals content a few percentages of errors, the control becomes jerky and even unstable resulting in poor converter reliability.



(a) AD8531 from Analog Device (b) OPA188 from Texas Instruments

Figure 2.3 Power supply rejection ratio of typical op-amps
(a) AD8531 Taken from Analog Device (2008)
(b) OPA188 Taken from TI (2016b)

The above examples show the fact that violating the voltage variation limits of the components can drive the power converter into an erratic control behavior resulting in poor reliability. Therefore, it is mandatory to control noise appearing in the low power circuit.

Due to the lack of literature about the research problematic, this chapter aims to answer the essential questions of noise in power converter: **"a) Does noise exist in low power circuit of power converter and b) where it comes from?"** This chapter provides the clearly observable evidences of noise in low power circuit and noise propagation from high power circuit to low power circuit by experimental results. In addition, this chapter also investigates the effects on noise spectra of different operating points of the high power circuit and impedance of components in the low power circuit by experiment. Based on the results shown in this chapter, the modeling approaches and noise attenuation methods will be introduced in the next chapters.

2.2 Experimental setup

2.2.1 Overall experimental setup

Noise measurement is a complex task. Consequently, it requires a well designed experimental setup to avoid incorrect results. In this section, a proposed experimental setup is explained in details. Since noise measurement is strongly related to the experimental setup, the converter is designed carefully to control the noise propagation paths and avoid unwanted noise sources. The standard Si-FET is used as the high power switch of the converter instead of SiCMOS to keep the gate driver circuit simple and convenient to analyze the noise propagation paths. Instead, the SiCMOS driver circuit contains the supported current amplifier circuit complicating the noise propagation paths to be determined (Cree, 2014) - (Avago, 2014). It is worth noticed that the commercial DC/DC converters are used in this experiment due to its compliance with industrial EMI standards. It is essential in the proposed experiment to avoid the unwanted noise created by a non-standard compliant DC/DC converter.

The purpose of the experiment is to measure noise in the low power circuit of the power converter during the switching transients of the power transistors. Since the low power circuit is linked to the power supply of the high power transistor's gate driver, the voltage probe's impedance may have significant influence on the results. Therefore, the current measurement method using current transformer is employed to avoid direct contact with the converter circuit. The results can be translated to the voltage spectrum by multiplying current spectrum with LISN impedance.

The experimental setup, shown schematically in Fig.2.4, is used to measure the current spectrum of i_n in the low power rail supplying the gate driver DC/DC converter DC1. The measurements are taken at several operating points of the high power circuit and low power circuit components.

The experimental setup is shown in Fig. 2.5, including:

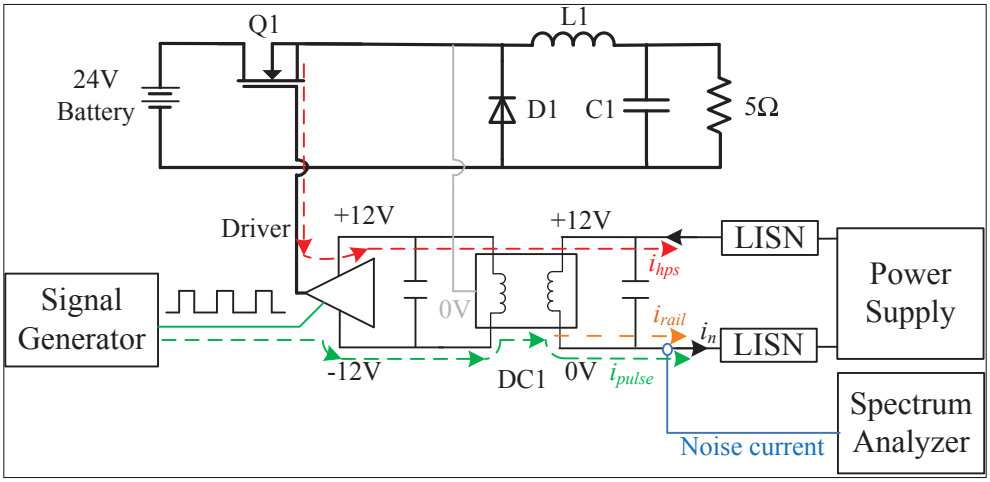


Figure 2.4 Schematic of the experimental setup for noise measurement

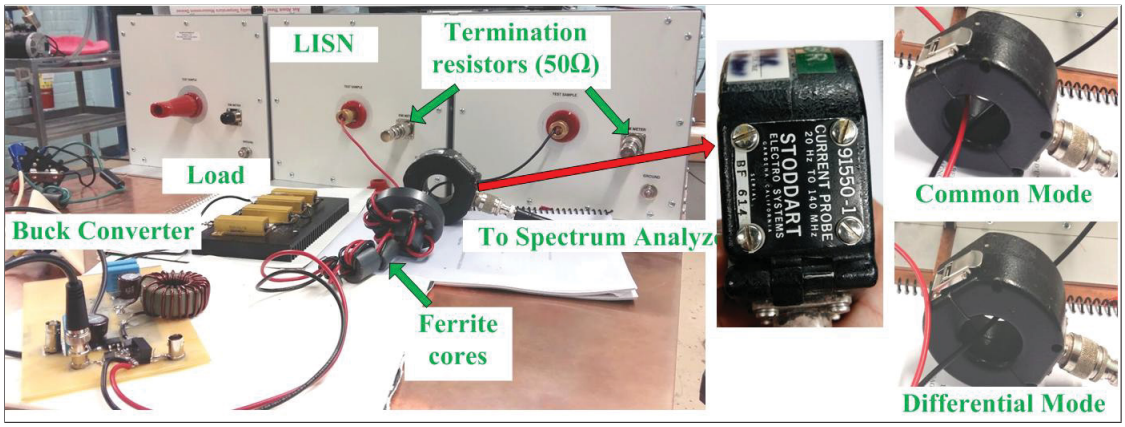


Figure 2.5 Complete noise measurement setup with
common mode current rejection by ferrite cores

- An experimental buck converter, which will be presented in Section. 2.2.2;
- An Agilent Signal Analyzer CXA N9000A to measure the current spectrum using the Current probe (Lindgren, 2008);
- Several ferrite cores are used in the winding of the cables prior to enter in the LISN to attenuate the CM noise from measurements. It is to ensure that the measured results for DM current is not affected by CM current. This practical method will be introduced in Sec. 2.2.3.

Fig. 2.5 also shows the way of measuring CM and DM current noise. DM current is measured on 1 line (positive or negative rail) whereas the CM current is measured on both 2 lines.

2.2.2 Buck converter designed for noise measurement

A basic Buck converter prototype is shown in Fig. 2.6. Its operating principle has been introduced in many documentations, so it is not presented here to keep the focus on noise measurement. The noise current is measured at the low power rail, typically $12V$, which supplies the input of the Gate driver DC/DC converter (DC1), whose outputs are typically $\pm 12V$. To avoid multiple noise sources and multiple propagation paths for noise in the setup, resulting in unknown results, the power supply for each part is chosen as below:

- The DC bus is supplied by a 24V battery bank consisting of 2 serial 12V batteries. Since noise in the current from the battery is negligible, there is no noise coming from the supply of the DC bus. In addition, the batteries are isolated from other devices used in the measurement, so their is no unknown propagation path for noise to travel to the low power circuit through those devices;

- The pulse driving the power switch, Q_1, is provided by a commercial signal generator to avoid the noise to propagate to the remaining parts of the low power circuit. In practical applications, the pulse signal is generated by a comparator of an analog controller or a digital micro-controller. For both devices, the power supply is generated from the low power rails, where noise is measured. This loop is a possible propagation path for noise in low power circuit, which complicates the analysis of the results;

- A commercial DC power supply to provide 12VDC rail to the input of DC1 via a 2-phase LISN. Each phase of LISN is terminated by a standard 50Ω resistor, resulting in 100Ω constant impedance of the DC power source over large frequency range. This selection ensures that their is no noise coming from the source of the power rails and impedance of the power source is constant.

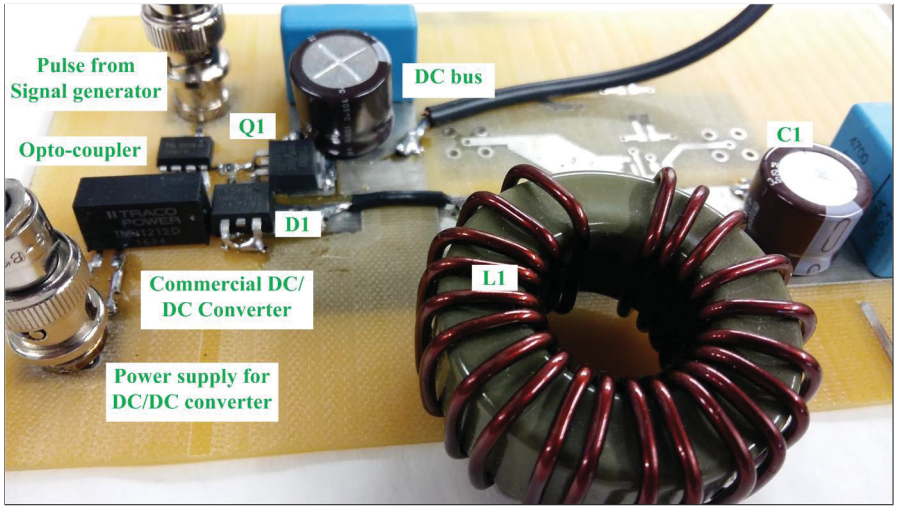


Figure 2.6 Prototype of a Buck converter used for noise measurement

Finally, there are 3 possible noise sources in the proposed setup, propagating to the power supply by the paths indicated in Fig.2.4:

- i_{rail} resulted from the voltage ringing due to switching operation of DC1;
- i_{hps} produced by the voltage ringing due to switching operation of Q1;
- i_{pulse} created by the input pulse of the Opto-coupler.

The noise current measured by the signal generator is the sum of 3 aforementioned currents.

2.2.3 Common mode noise rejection

Noise measurement on a cable can consist of CM and DM noise with significant contribution of CM. It is difficult to analyze the noise propagation paths corresponding to each mode. Thus, removing CM while measuring DM current is necessary to properly analyze the obtained noise spectrum. Taken into account the cables used to connect the input of DC1 to the LISN, as illustrated in Fig. 2.5, the equivalent impedance seen from the power transistor to the power supply for the low power circuit is shown in Fig. 2.7. In this figure, the DC/DC converter is

represented by its isolation capacitance. In order to reduce CM current, a practical method is using common chokes to increase the CM impedance of the cables.

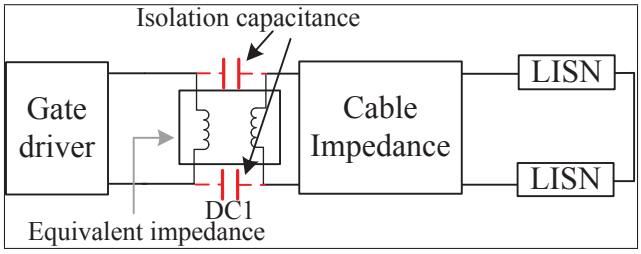


Figure 2.7 Equivalent impedance seen from power transistor to low power circuit supply

In this approach, the cable CM impedance is increased by winding positive and negative rails together on the ferrite cores. Considering the fact that each ferrite core is effective on a limited bandwidth, several cores are used in series to increase the CM impedance of the cables over the considered frequency range (100kHz - 140MHz), as shown in Fig. 2.8. This figure also shows the cable impedance measurement setup with the Vector Network Analyzer (VNA) Agilent E5061B using the method called port 1 reflection, which is accurate for high bandwidth (up to 3GHz) and mid-impedance level (Keysights, 2017). Prior to take the measurements, the device is calibrated using open, short and load (standard 50Ω) calibration procedure.

The CM impedances of the cable with and without the ferrite cores are shown in Fig. 2.9. One observes a significant increase of the CM impedance with the effect of ferrite cores compared to the case without ferrite core, especially in the frequency range of 100kHz - 60MHz. In the frequency range over 60MHz, the CM impedance of the cable without ferrite cores is higher due to the transmission line effect. The total of DC1 isolation capacitance and CM impedance of cable for both cases with and without ferrite cores are also plotted in Fig.2.9. It is the impedance seen from the high power transistor to the +12V rail power supply of the low power circuit while neglecting the stray inductance in the gate driver circuit. This assumption is valid since the stray inductance is very small compared to the CM impedance of long cables used

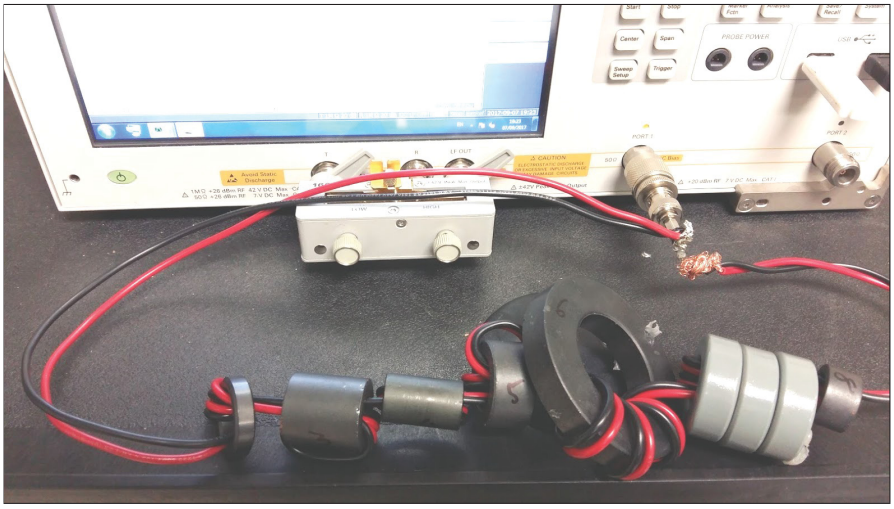


Figure 2.8 Ferrite cores to remove CM current

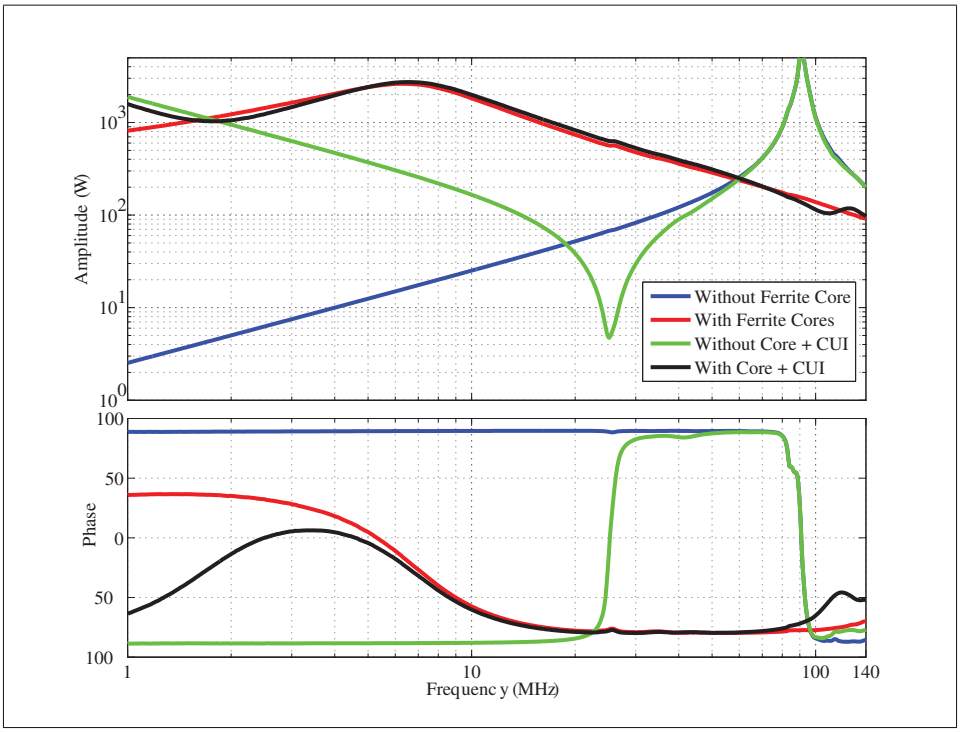


Figure 2.9 CM impedance of the cable with different combinations

in measurement, especially with ferrite cores. Thus, it is interesting to analyze the mentioned total impedance with the CM current spectrum obtained from measurement.

One observes the same impedance for both cases in the frequency range below 2MHz due to the high impedance of the isolated capacitance of DC1. The ratio between these two impedance increases logarithmically in the frequency range of 2MHz - 25MHz and reaches the highest difference of 40dB at 25MHz. This trend is reflected in the CM noise current spectra shown in Fig. 2.10, where the noise attenuation increases up to 30dB at 25MHz.

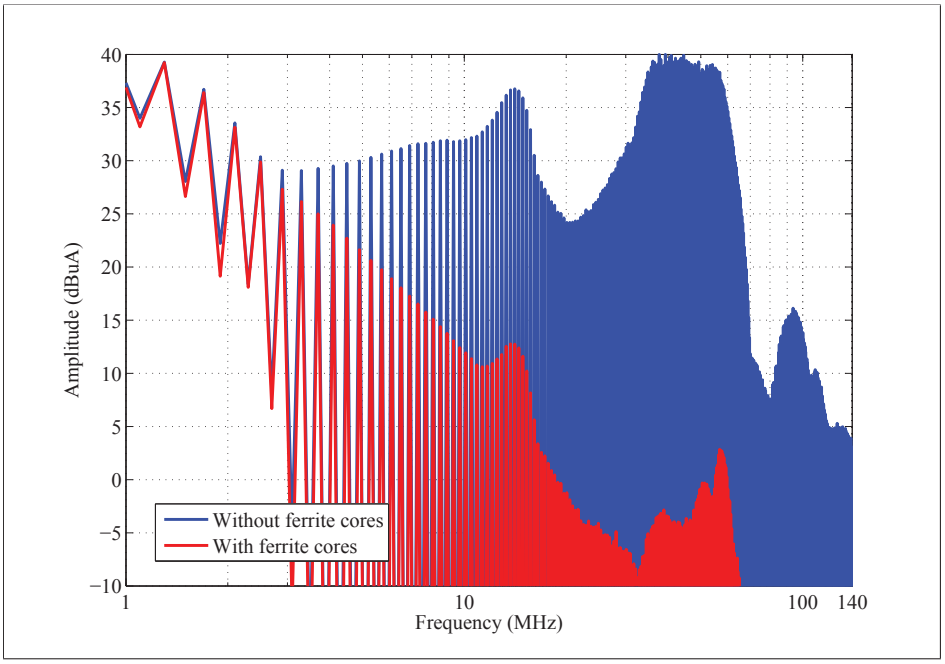


Figure 2.10 CM current spectrum with and without ferrite cores on the cable

In the frequency range over 25MHz, noise without ferrite cores is higher than that at lower frequency range since its impedance becomes inductive with positive phase, which provides an ideal path for noise to travel. Instead, the impedance with ferrite cores is capacitive with negative phase, providing barriers for noise to propagate As a result, the attenuation obtained with the ferrite cores is about 30 - 40dB in this frequency range. This significant attenuation confirms the effectiveness of the ferrite cores to attenuate CM noise in the cable.

2.2.4 Isolation capacitance measurement

As pointed in Sec. 2.2.3, the isolation capacitance, which is the capacitance between the input and output, of the DC/DC converter, including its amplitude and phase, has a significant contribution on the noise spectrum. The positive phase can increase noise propagation despite of its very high amplitude. Therefore, the actual impedance curve with parasitic inductance is more important than only the capacitance value, which is the only information being received from the manufacturer. The only way to accurately obtain the isolation capacitance is to extract it experimentally, as shown in Fig. 2.11. In this measurement, the pins at the input side are shorted together, as well as the pins at the output side. The impedance is measured between 2 sets of input and output pins.

Figure 2.11 DC/DC converter isolation capacitance measurement

Table 2.1 List of commercial DC/DC converters used as Gate driver supply

Manufacturer	Part Number	Description	Isolation Capacitance
TRACO	TMH 1212D	2W 12VIN +/-12VOUT	$80pF$
CUI	VASD1-S12-D12-SIP	1W 12VIN +/-12VOUT	Not mentioned
RECOM	RD-1212D	2W 12VIN +/-12VOUT	$40pF$ - $115pF$

In the experiments, 3 commercial DC/DC converters are used. These devices are summarized in Table 2.1. Their isolation impedances are shown in Fig. 2.12. As can be seen, all isola-

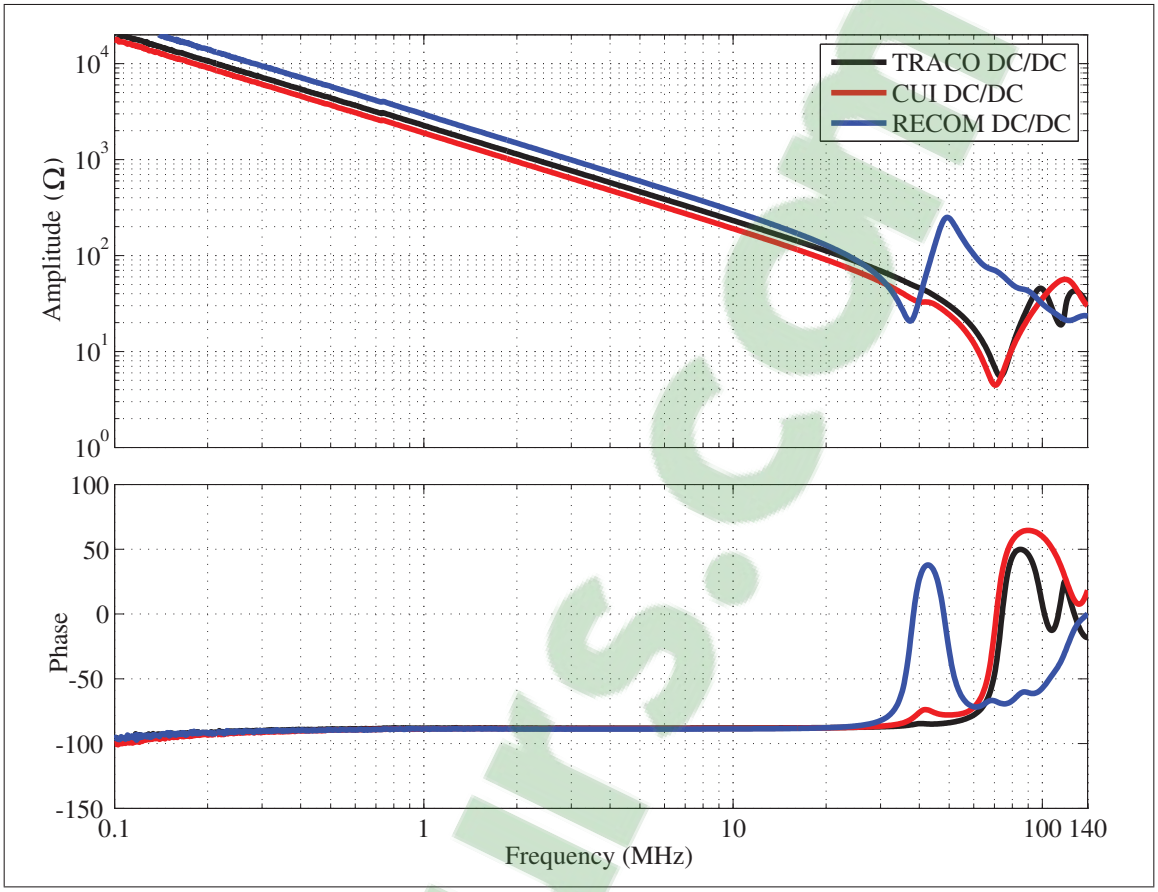


Figure 2.12 DC/DC converter isolation capacitance

tion impedances are very high up to 30MHz. There are two corner frequencies of 35MHz and 50MHz in the RECOM DC/DC impedance with positive phase within this frequency range. The isolation impedance of the TRACO DC/DC and CUI DC/DC are similar with corner frequencies at 70MHz and 75MHz, respectively. From these impedances, one expects different noise spectra between a converter built with RECOM DC/DC and TRACO DC/DC or CUI DC/DC. An experiment to compare these two cases will be presented in Sec. 2.3.2.

2.3 Experimental results

In this section, experimental results of noise measurements on the converter introduced in the previous sections are presented. The measurements are taken under different operating conditions of the high power circuit and for different components of the low power circuit. Through

the comparisons, one observes the influences of each factor in the noise spectrum. Based on these experimental observations, more details about sub-research topics will be presented in the next chapters of this thesis. Table 2.2 shows the common experimental characteristics used in the following sections. Some variables will be changed for specific measurements for comparison purpose.

Table 2.2 List of experimental characteristics

DC Power Supply	Load	Switching frequency	Duty Cycle
24V	5Ω	100kHz	60%

2.3.1 Effect of power transistor switching operating on noise spectrum in Low power circuit

In order to investigate the effect of the high power transistor operation on the low power circuit, the DM and CM current at the input of the DC1 are compared for the following cases. The descriptions are given in Figs. 2.14 and 2.15, showing the spectra of CM and DM noise current at the input of Gate driver DC/DC converter, respectively.

Case 1: *Rail supply*: 12V is supplied to the input of DC1. This case is to measure the noise generated by DC1 due to its switching operation, $i_n = i_{rail}$, as shown in Fig. 2.13a.

Case 2: *Pulse Signal + Rail supply*: 12V is supplied to the input of DC1, pulse is applied to the input of the Opto-coupler. This case is to used to study the effect of the Q1 switching operation without load current on input of DC1 via the Opto-coupler, $i_n = i_{rail} + i_{pulse}$, as shown in Fig. 2.13b.

Case 3: *High power switch + Pulse Signal + Rail supply*: 12V is supplied to the input of DC1, pulse is applied to the input of Opto-coupler, the main DC bus is supplied by Battery bank. The power is transferred from the battery bank to the load through the converter. This experiment

is performed to investigate the effect of Q1 switching operation with load current on the input of DC1, $i_n = i_{rail} + i_{pulse} + i_{hps}$, , as shown in Fig. 2.13c.

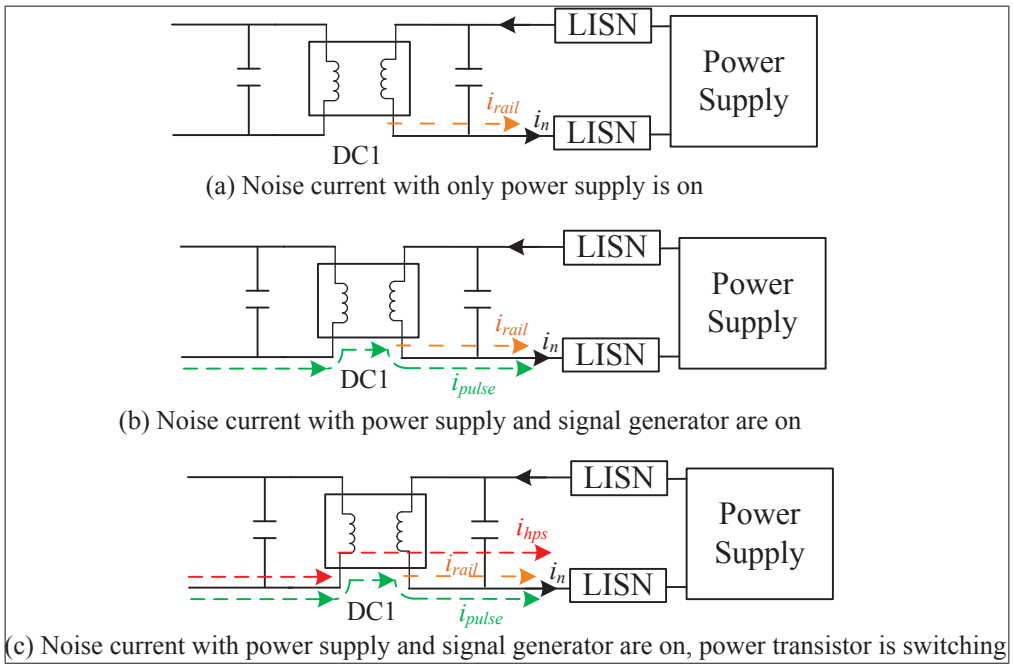


Figure 2.13 Noise current of operation of difference devices

As shown in Figs. 2.14 and 2.15, the noise generated by DC1 (red) decreases with frequency, below $-10dB\mu A$ at frequency of 10MHz. This current in the rail supply is created by the switching operation of DC1. In addition, the noise injected from the pulse of the Opto-coupler (blue) is negligible since the noise spectrum of Case 1 is mostly same as that in Case 2. It can be explained by the very low current at the input (about 10mA to turn on LED inside the opto-coupler) while the isolated impedance via the opto cell is very high.

On the other hand, the noise spectrum is significantly increased when the high power switches operates. For instance, the noise current is increased by few dB to $10dB$ in 100kHz to 2.5MHz frequency range and more than $20dB$ in frequency range higher than 3MHz. It proves the significant contribution of noise propagation from the high power circuit, i_{hps}, in the noise at the low power circuit.

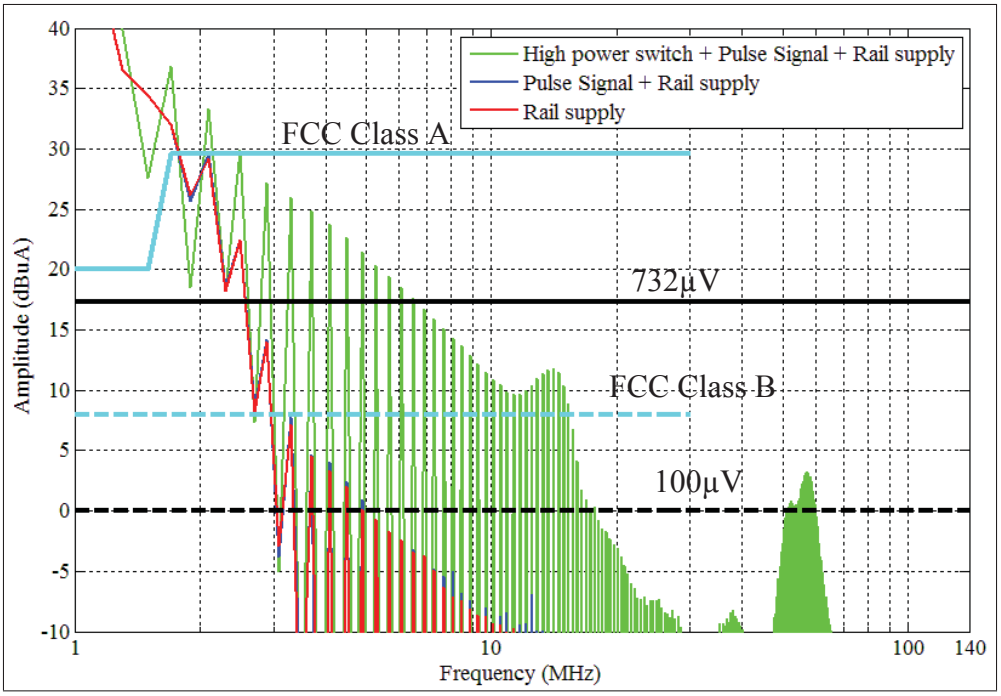


Figure 2.14 CM noise spectrum with TRACO DC/DC converter

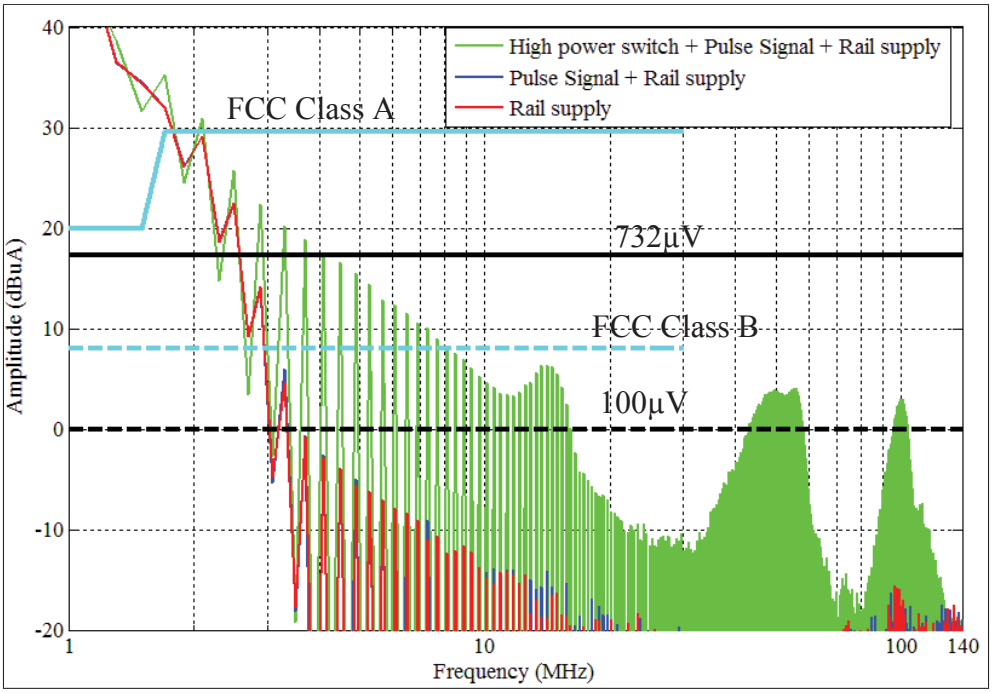


Figure 2.15 DM noise spectrum with TRACO DC/DC converter

In these figures, the equivalent noise current limit of the EMI standard FCC Class A and B are also plotted by translating the voltage level limits via the LISN impedance ($100\Omega = 40dB\Omega$ in this setup). It must be noticed that FCC standards are used as the limits of EMI at the input of high power circuit, not the low power circuit. However, since there is no standard existing for low power circuits, it is important to understand if this noise spectrum is acceptable. Therefore, these standards are used in as the references for comparison purpose. For the same reason, the limits of $732\mu V$ and $100\mu V$ for DSP mentioned in Sec. 1.1 are also used in this figure. As seen, the noise current exceeds the FCC Class A at frequencies below 2MHz and FCC Class B in the frequency range of 0.1MHz - 15MHz. Also, the limit of $732\mu V$ is exceeded by the CM and DM in frequency up to 7MHz and 4MHz, respectively. On the other hand, the limit of $100\mu V$ is violated by the CM and in the frequency range of 0.1MHz - 15MHz and 50 - 60MHz. Since the current spectra exceed limits for several occurrences when the high power switching operates, it can easily degrade the performance of the converter.

The significant impact of high power circuit switching operation to the low power circuit in term of current spectrum is essential for the research of noise propagation in power converters presented in this thesis. The results in this section are the evidences of the noise source while the noise spectrum, which exceeds several limits, shows the potential impact of noise on the converter reliability. Therefore, it is mandatory to consider noise issues in the low power circuit in the design process to guarantee the power converter performance.

2.3.2 Effect of Gate driver DC/DC converter isolation capacitance on noise spectrum in low power circuit

As pointed in Sec. 2.3.1, a significant noise current is injected from the high power circuit to the low power circuit. In the experimental setup presented in this Chapter, the only propagation path is the isolation capacitance of DC1. In this section, the effect of this isolation capacitance on noise current in the low power circuit is investigated by comparing the current spectra of the converter with different commercial DC/DC converters used as DC1.

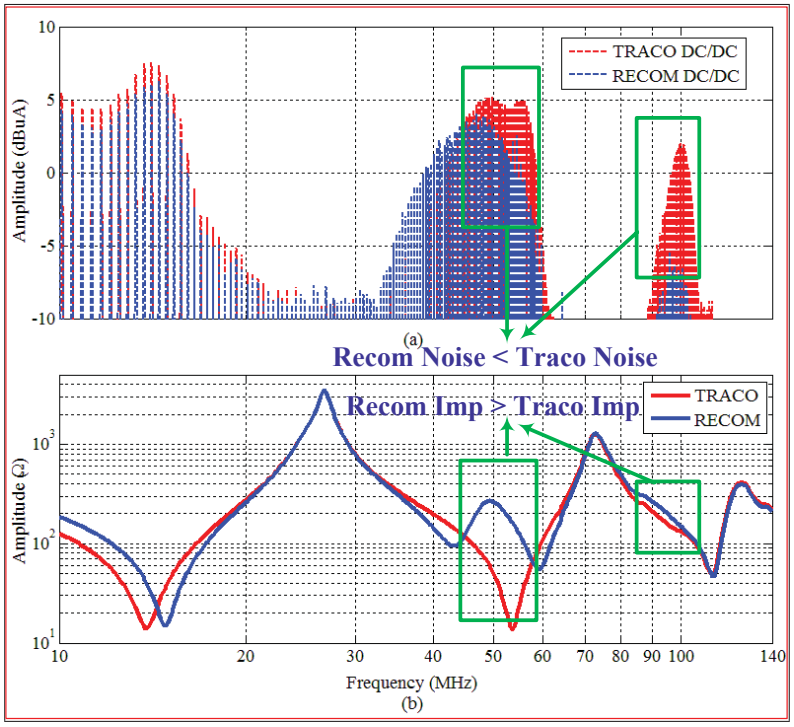


Figure 2.16 (a) DM current with different DC/DCs
(b) Equivalent impedance (DC/DC + cables)

The comparison of CM current spectra between the Buck converter using RECOM and TRACO DC/DC as the Gate driver supplies are shown in Figs. 2.16 and 2.17. These two figures show the same contents of current spectra with different color sequences to clearly distinguish the current spectra in different frequency ranges. The impedance shown in Figs. 2.16b and 2.17b is the total impedance of DC1 isolation capacitances and the DM impedance of the cables used in measurement which is extracted by the measurement setup introduced in Sec. 2.2.3. It is observed that the lowest current spectra in the frequency ranges of 20-35MHz and 60-90MHz correspond to the highest impedance of the total DM impedance.

Also, it is clearly shown in Fig. 2.16a. that the current spectrum of the RECOM DC/DC is $5-10dB$ higher than the TRACO DC/DC in the frequency ranges of 45-55MHz and 80-110MHz. There is also a minor difference of $2-3dB$ in frequency range of 10-15MHz. This is caused by the higher equivalent impedance, including the isolation capacitances of the RECOM DC/DC and the cables, in the corresponding frequency ranges, as given in Fig. 2.16b.

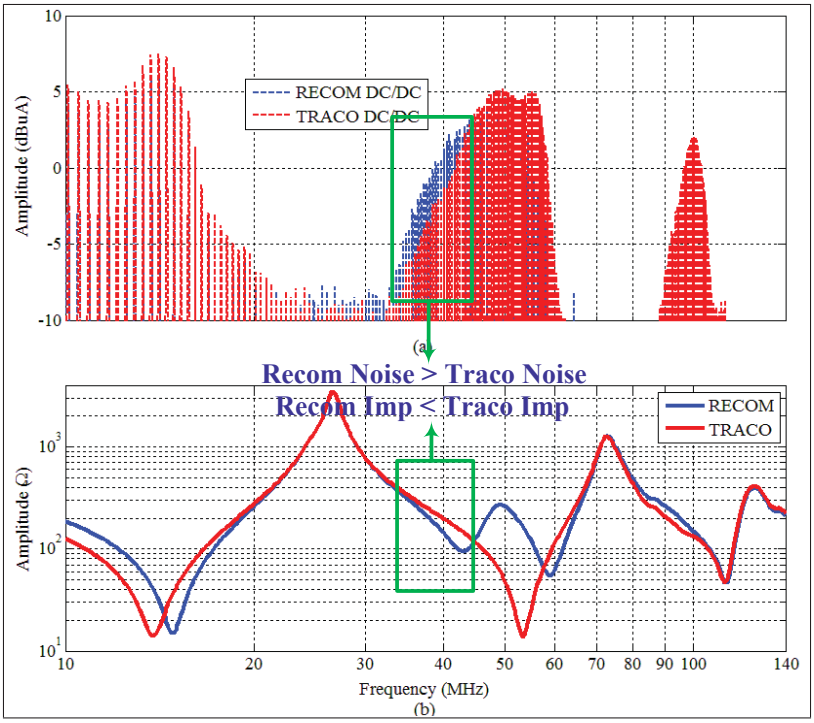


Figure 2.17 (a) DM current with different DC/DCs
(b) Equivalent impedance of DC/DC + cables

Its contrastive comparison is observed in Figs. 2.17a and b in frequency range of 35-45MHz. These results clearly show the link between the impedance of different commercial DC/DC converters, surrounding impedance and the noise spectrum. It is important to notice that the isolation capacitance of the DC/DC converter alone doesn't correlate directly the noise profile, but its interaction with the surrounding impedances. This fact is the motivation to conduct research on the impedance modeling of the surrounding components such as the passive components, presented in Chapter 3, and the low power rails, presented in Chapter 4.

2.3.3 Effect of duty cycle of power transistors on noise spectrum in Low power circuit

To analyze the effects of high power transistor duty cycle on the noise performance in the low power circuit, the current spectra of i_n are shown with different duty cycles of Q1 in Fig. 2.18. One observes the different current spectra in the frequency ranges of 10MHz - 15MHz and 40MHz-60MHz, and similarity in the remaining bandwidth.

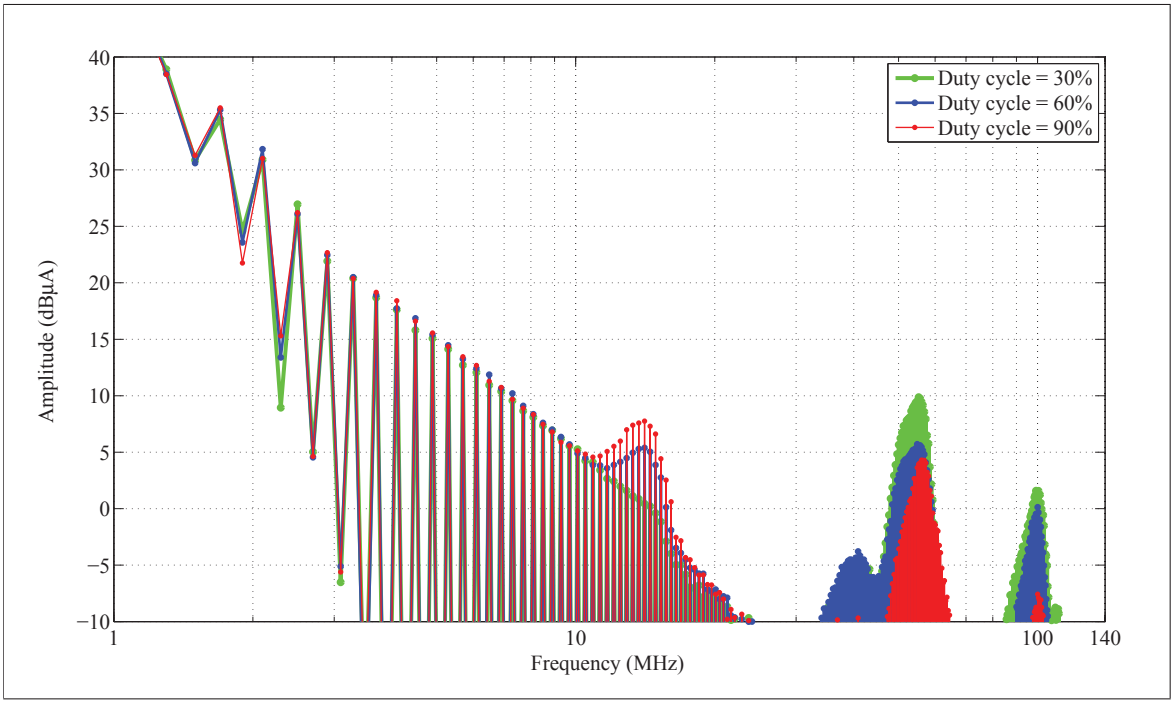


Figure 2.18 DM current spectra with CUI DC/DC converter, switching frequency of 120kHz

In the frequency range of 10MHz - 15MHz, DM current spectra decrease with the duty cycle. It can be explained by the fact that noise in this frequency range is created by the rising edge of the power switch and depends mainly on the average DC bus current. Higher duty cycle corresponding to higher DC bus current resulting in higher noise.

In the frequency range of 40MHz - 60MHz, the current spectrum decreases while the frequency increases. These observations will be analyzed and explained more deeply in Chapter 5.

2.3.4 Effect of switching frequency on noise spectrum in low power circuit

To observe the effect of the switching frequency of high power transistors on noise in low power circuit, the DM current spectra at the input of DC1 are measured with different switching frequencies of Q1 such as 50kHz, 100kHz and 140kHz whereas all other conditions are the same.

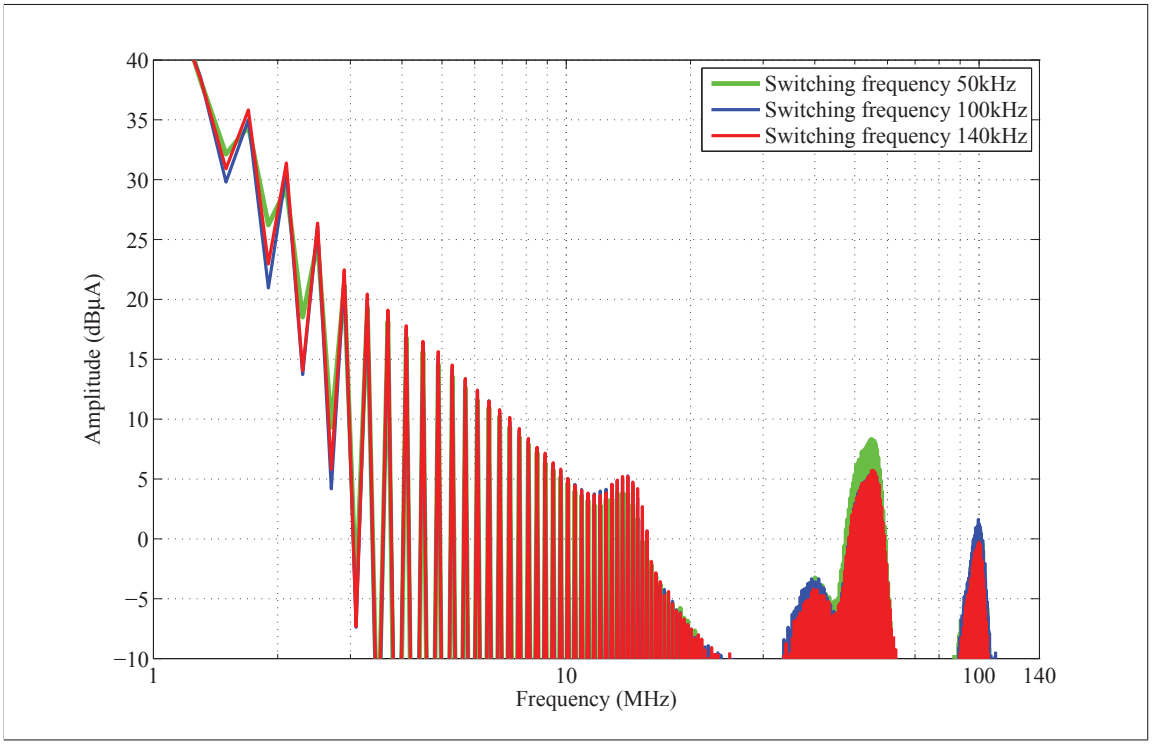


Figure 2.19 DM current spectra with CUI DC/DC at different switching frequencies

The current spectra are shown in Fig. 2.19 in frequency range of 1MHz to 140MHz. Two observations on the current spectrum performances can be made:

- In the frequency range from 1MHz to 3MHz, the DM current at switching frequency of 50kHz is slightly higher than the others. It is because noise in low power circuit is mainly caused by the switching current ripple on the DC bus and its multiple harmonics while the current ripple is higher at lower switching frequency with the same converter components, specifically line inductance and output capacitance. It is also observed that there is no difference between noise spectra for 100kHz and 140kHz switching frequencies;

- In the frequency range from 3MHz to 140MHz, DM current of the three cases are the same. It is reasonable since the noise in high frequency depends on the voltage ringing V_{DS} at the transient states of the high power switch. This voltage ringing is related to the rising/falling time and instantaneous line current which depends on the transistor peak current.

These results show that DM noise current in the low power circuit is mostly independent on the switching frequency of the high power switches.

2.4 Conclusion

In this chapter, the noise propagation in a power converter from high power circuit to its low power circuit has been introduced. The specific experimental setup of a Buck converter for noise measurement has been presented. The experimental results show the effects of several factors on noise transmitted to the low power circuit. They are summarized as follows:

1. There is significant noise injected by the high power switching operation to the low power circuit while the high power switches are operating. This noise source must be considered during the converter design process;

2. Even though parasitic capacitance of the commercial DC/DC converter used as Gate driver supply is usually low, its interaction with the surrounding impedance can create low impedance path at some frequency ranges, allowing noise to propagate easily into the low power circuit. Due to the importance of the surrounding impedance, impedance modeling of the components such as passive devices (common choke, filter, transformer, etc), and low power plane (the common plane supplying voltage for all low power circuit), are mandatory to quantify noise in low power circuit. These results lead to the research on modeling of passive devices and low power plane, presented in Chapters 3 and 4, respectively;

3. The switching frequency of the high power transistor doesn't have effect on the noise propagation to the low power circuit at high frequency (over 10MHz). In this frequency range, noise is created by the voltage ringing across drain - source of the power transistor at transient states (rising and falling edges of V_{DS}) during its switching transients. These voltage ringing amplitudes depend on the impedances of the power transistor and gate driver, not related to the switching frequency. How the interaction between these impedances influences noise in low power circuit and how to attenuate noise in this frequency range are important to complete noise study. These topics will be presented in Chapter 5 with noise

analysis in addition to a practical method to attenuate noise at specific frequencies based on Y-capacitor utilization;

4. The duty cycle applied to high power switch has an effect on noise performance in conducted EMI frequency range due to its direct relation with the average current. This relationship will be explained by the researched presented in Chapter 5.

CHAPTER 3

GENERAL IMPEDANCE REPRESENTATION OF PASSIVE DEVICES BASED ON MEASUREMENT

Motivation

As presented in Chapter 1, passive components, i.e. filter, capacitors, inductors, transformers, ferrite beads, etc, are the fundamental parts of the power converter. Therefore, their impedance models are essential to predict noise propagation in both high power and low power circuits of the converter. Due to the fact that most of available impedance measurement devices are designed to measure 2 - port components, measuring impedance of 2 - pin components such capacitors, inductors and ferrite beads needs proper measurement devices and techniques. However, measuring multiple-port components such filters, transformer and other *black-box* components requires more complex techniques and mathematical tool to translate the measurement results of 2 - port impedance to a multiple - port model. It is motivated to develop a new modeling approach for general passive devices which will be introduced in this chapter.

Summary

Noise propagation from power stages of power converters to their low voltage control boards depends on multiple complex paths, generally created by parasitic capacitors across isolation barriers. These barriers can be easily cross by the high frequencies (up to 100MHz (Oswald *et al.*, 2014)) generated by new semiconductor technologies such SiC and GaN resulting in compromised signal integrity on the control side. A common approach to overcome this problem is by using filter. However, due to the presence of several complex propagation paths, DM and CM modes are not properly defined at board level, causing difficulties to predict filter's performance. To cope with this issue, the node-to-node impedance function (NIF) is proposed to identify the impedance of all possible propagation paths in the filter. In the considered frequency range (>30MHz), NIF parameters identification precision is altered by the impedance of shorting paths used in measurement procedure. In this chapter, an optimization procedure

based on Newton-Raphson algorithm is proposed to remove these errors. This improved version of NIF is named General Impedance Representation (GIR). Thanks to its generality, the GIR can also applicable for all kinds of passive devices. Experimental results are presented to confirm the effectiveness of GIR.

The content of this chapter was published on *IEEE Proceeding of ICIT 2017* and *IEEE Transaction of Power Electronics* in September 2017 (Nguyen *et al.*, 2017a).

3.1 Introduction

The incoming of SiC and GaN technologies in power conversion bring several benefits such improved power density and higher efficiency. However, high switching frequency (hundreds of kHz to MHz) combined with short rise and fall times of SiC and GaN devices produce higher EMI than standard Si-based converters, as pointed in Section. 2.1.

In addition to increasing the noise on the power leads, these high frequency currents will travel more easily across the multiple insulation barriers inside the converter, as shown in the simplified example of Fig. 3.1. In this example, one observes parasitic capacitors in parallel with the insulation of the gate driver DC/DC converter (C_1 and C_2) as well as the parasitic capacitor (C_{CM}) between the low power rails of the converter and the heatsink. These capacitors create unexpected propagation paths for the noise generated by the power stage to the surrounding circuits and more precisely the low voltage power rails. These low voltage power rails are used to supply semiconductors dedicated to control such as DSP and analog circuits. These circuits are very sensitive to the quality of their supply and malfunctions can arise if voltage spikes are present in the rails, decreasing the converter reliability (Nguyen *et al.*, 2017c). Therefore, the noise level propagated from the power stage to the low power rails must be under control. A common approach to overcome this problem is by integrating filters between these two parts of the converter.

A difficult question arises at this point. The basis of this questioning is illustrated on Fig. 3.1a. The propagation path i_{dm} is considered as the DM noise from the filter point of view, without

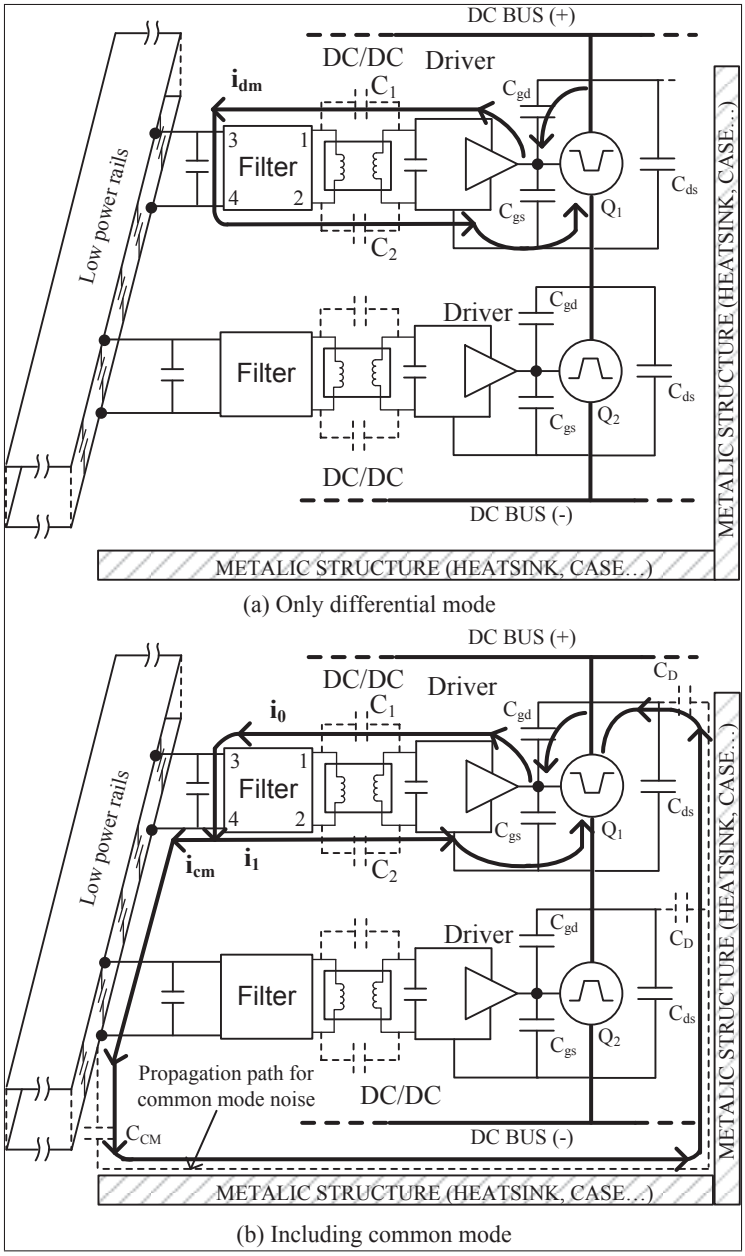


Figure 3.1 Basic noise paths in a power converter

considering the effect of the metallic parts (case, heatsink) of the converter. However, noise propagates in multiples other paths as shown by propagation paths i_{cm}, and i_1 on Fig. 3.1b with the presence of the parasitic capacitance between the heatsink and low power rails (C_{CM}), and switching devices (C_D). This simplified example shows that the formal DM and CM definitions

are difficult to interpret from the filter point of view. In fact, noise can travel from any pin of the filter to any other one.

The proposed approach to cope with this ambiguous current distribution is the NIF black-box-model modeling shown in Fig. 3.2 (Nguyen *et al.*, 2017b; Liu *et al.*, 1993). This modeling approach doesn't assume DM or CM noise but provides propagation path impedance between each pin of the filter. Also, NIF provides a good insight of filter weakness and performance in the frequency domain. Finally, NIF modeling is general and it can be effectively used for all passive devices, such as common chokes, on-board transformers, planar structures, etc. However, even though the NIF is a powerful tool to understand the filter's performance, its impedance identification is altered in EMI frequency due to complex interaction between impedance of devices and shorting paths used in impedance measurement procedure. Consequently, the main contribution of this chapter is to extend the validity of NIF models in a large frequency bandwidth (from 100kHz to 200MHz). The resulting improved impedance representation is called GIR (General Impedance Representation). Since it has been shown that off-line impedance of the passive parts of the power converter are useful to precisely predict EMI of a power converter (Rondon-Pinilla *et al.*, 2014; Han *et al.*, 2017b; Brovont & Pekarek, 2017), this contribution will help to improve EMI filter characteristics for the next generation of power transistors such as SiC and GaN.

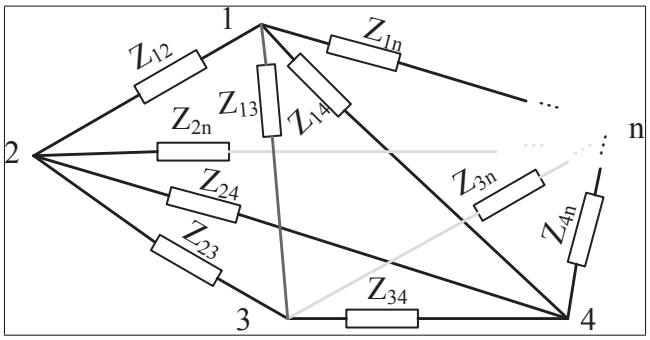


Figure 3.2 Equivalent circuit of a n-pin passive device

The chapter is organized as follows. In Sec. 3.3, the measurement procedure to build GIR model is presented. It is followed by the analysis of the impact of the shorting path impedance on the connecting impedance computation in Sec. 3.4. In Sec. 3.5, an optimization procedure based on Newton-Raphson is presented with the required assumptions to ensure the accuracy and convergence of the algorithm. Finally, Sec. 3.6 provides the experimental results of a commercial LC filter followed by the conclusion in Sec. 3.7.

3.2 Passive components modeling and impedance extraction

In the literature, passive components have been modeled by using computational and measurement-based methods. Computational methods are employed for designing devices such as FEM (Kovačić *et al.*, 2015) and PEEC (Kovačević *et al.*, 2014) based on device geometry and materials. These methods have great advantages but they are not able to handle commercial *black-box* devices where all components are integrated and covered in a case.

Measurement-based methods are the answer to this issue. For these methods, a set of impedance measurements is performed to determine all the elements of a given theoretical model such as transformers (Filipović-Grčić *et al.*, 2015; Kim *et al.*, 2016) and common mode chokes (Sánchez *et al.*, 2010; Deng & See, 2007; Kovačić *et al.*, 2012; Stevanovic *et al.*, 2013; Tan *et al.*, 2013; Cuellar *et al.*, 2016; Nomura *et al.*, 2016; Illia *et al.*, 2017; Messo *et al.*, 2016). Advanced common choke models taken into account the complex permeability (Nomura *et al.*, 2016) and core saturation under bias conditions (Illia *et al.*, 2017) have been recently developed. An online impedance measurement method of the common choke based on the performance of the common mode current was introduced in (Messo *et al.*, 2016). However, the limit frequency range of 25kHz, which is not sufficient for modeling in the EMI frequency. Scattering parameter measurements are used to extract the model of planar LC filter (Wang *et al.*, 2014). Although the results are good, this approach still needs a pre-defined model that is not available easily for many parts.

The NIF models are developed in (Nguyen *et al.*, 2017b; Liu *et al.*, 1993),(Gustavsen, 2004, 2016; Stevanović *et al.*, 2014; Marlier *et al.*, 2015) to cope with the unknown pre-defined model devices. In this modeling approach, each pin pair are linked together by a connecting impedance, as shown in Fig. 3.2. The connecting impedance is computed from the data obtained by measurements. Since the impedance is measured in frequency domain, all frequency - dependent parameters (such as permeability and skin effect) are embedded in the measured data.

3.2.1 Impedance Extraction

Although measurement-based methods are attractive due to their generality, experimental impedance extraction is an important topic by itself. A survey of this topic is presented hereafter. There are two impedance measurement methods that can be employed: direct or indirect measurement.

The direct measurement method is employed in (Gustavsen, 2004) using Vector Network Analyzer (VNA) with an auxiliary connection board, including current sensor and jumpers-to-ground, to measure the admittance matrix of a power transformer. The errors caused by measurement cables are eliminated by taking its transmission line model into computation (Gustavsen, 2016). The other direct methods are introduced in (Stevanović *et al.*, 2014) - (Marlier *et al.*, 2015) for the cables. In (Stevanović *et al.*, 2014), the connecting impedance matrix is converted from the S-parameters measured on the short circuit and matching load configurations. It is not applicable for general devices with unknown matching load of pins. In (Marlier *et al.*, 2015), the guarding technique of Impedance Analyzer (IA) is exploited to measure the connecting impedance. In this technique, two measured pins are connected to the High and Low terminals whereas the non-measured pins are shorted to the *guard terminal* while neglecting the impedance of connecting paths.

The indirect measurement method using IA was introduced in (Liu *et al.*, 1993). In this approach, the pins of the devices are divided into 2 groups, pins in each group are shorted together. The impedance is measured between two groups to write a linear equation for the connecting

impedance variables. This procedure is repeated until a complete set of equations is obtained. The impedance matrix is then computed by a simple matrix inversion.

The two measured-based methods in (Liu *et al.*, 1993) and (Marlier *et al.*, 2015) are applicable for unknown matching load devices, but they are limited on the computing approaches of connecting impedance. These computing methods are based on the assumption of zero shorting path impedance, which is not always valid. In fact, this assumption is valid for specific applications where the impedance of the target devices, i.e. transformer and cables, are more inductive and less capacitive than that of the shorting paths. However, it is no longer valid for several passive devices such as small common mode chokes, EMI filters, on-board transformers or other devices with capacitive ports. There is a variety of connecting impedance which can interact with that of the shorting paths in EMI frequency leading to modeling errors, and hence, wrong EMI propagation models to study the power converter noise spectrum.

As pointed before, the main contribution in this chapter is to improve connecting impedance accuracy by removing the errors caused by the shorting path impedance. This chapter also contributes on the measurement approach by introducing the measurements of VTG and *open impedance* for accurately extracting the connecting impedance and verification purposes. It is important to emphasize that even though the measurements are taken off-line in this chapter, it doesn't mean that the proposed GIR is only effective for off-line impedance. Also, shorting impedance problems need to be overcome, whether the device is under bias or not.

3.3 GIR Approach

In this section, the analytical equations and measurement procedure of GIR based on NIF model (Liu *et al.*, 1993) is summarized to introduce the connecting impedance and the method of taking measurements.

A passive device can be represented by a general impedance matrix, as shown in Fig. 3.2. In details, each pin is connected to each of the others by a connecting impedance. For instance, for a

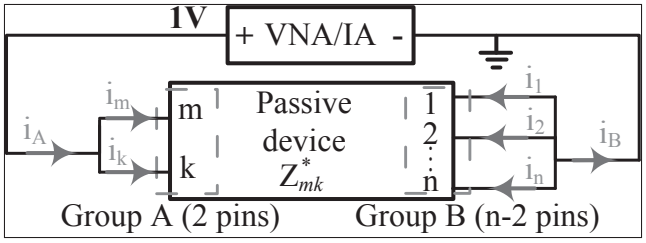


Figure 3.3 Group - impedance measurement by VNA

n-pins device, pin 1 is connected to pins $2,3,\ldots,n$ by impedance $Z_{12},Z_{13},\ldots,Z_{1n}$, respectively. In this definition:

- $Z_{ij} = Z_{ji}$ for all i, j;
- There are $C_n^2 = n(n-1)/2$ connecting impedances.

The Kirchoff's current law equation at all pins is:

$$\begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_n \end{bmatrix} = \begin{bmatrix} \sum_{i\neq 1}^{n} Y_{i1} & -Y_{12} & \cdots & -Y_{1n} \\ -Y_{12} & \sum_{i\neq 2}^{n} Y_{i2} & \cdots & -Y_{2n} \\ \vdots & \vdots & \ddots & \vdots \\ -Y_{1n} & -Y_{2n} & \cdots & \sum_{i\neq n}^{n-1} Y_{in} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_n \end{bmatrix} \tag{3.1}$$

where $Y_{ij} = 1/Z_{ij}$ is the connecting admittance.

Equation (3.1) shows the fact that all Y_{ij} can be calculated with given v and i. However, they cannot be measured simultaneously by a two - port VNA/IA. Thus, n pins of devices are grouped into 2 groups namely Group A and B. Assuming that pins in each group are shorted together with zero impedance shorting paths, all of them share the same voltage level; then, the n-pins device can be considered as a $2-$pin device whose impedance seen from A and B, hereafter called *group - impedance*, can be measured by $2-$port VNA/IA. Fig. 3.3 shows an

example of grouping and impedance measurement methods of a n-pin device where Group A contains pins numbered m and k, group B contains the remaining pins.

Considering VNA/IA as a normalized 1V voltage source without losing generality, the basic circuit elements are:

$$v_m = v_k = 1; \quad v_{i,i\notin\{m,k\}} = 0; \tag{3.2}$$

$$Y^*_{mk} = 1/Z^*_{mk} = i_m + i_k \tag{3.3}$$

where Z^*_{mk} and Y^*_{mk} is the measured impedance and admittance seen from A and B, respectively.

Replacing (3.2) and (3.3) into (3.1) yields:

$$Y^*_{mk} = \sum_{i\notin\{m,k\}}^{n} (Y_{im} + Y_{ik}) \tag{3.4}$$

(3.4) is an equation used to solve Y_{ij} once Y^*_{mk} is measured. For a n-pins device, there are C_n^2 variables which require C_n^2 independent equations to solve. Thus, the procedure of selecting m and k is repeated until C_n^2 equations are completed. Note that the number of pins in each group can vary from 1 to $(n-1)$, and the independence of the selected set of equations must be satisfied. The connecting admittance matrix is computed as:

$$\mathbf{Y_n} = \mathbf{C_n^{-1}} \mathbf{Y_n^*} \tag{3.5}$$

where $\mathbf{C_n}$ is the connecting matrix; $\mathbf{Y}^*_n$ and $\mathbf{Y}_n$ are admittance matrices that are measured and calculated, respectively.

3.4 Non-zero impedance shorting paths analysis

In this section, the connecting impedance identification procedure of a 3-pin device is investigated with the shorting path impedance. There are three impedance measurements taken following the procedure introduced in Fig. 3.4. By including the shorting path impedance ΔZ,

corresponding to an admittance ΔY, the equivalent circuits are shown in Fig. 3.5. The measured admittance is computed as follows:

$$\begin{aligned}
\tilde{Y}_1^* &= \underbrace{Y_{12}+Y_{13}}_{Y_1^*} - \underbrace{\frac{Y_{13}^2}{\Delta Y_{23}+Y_{13}+Y_{23}}}_{e_1^*} \\
\tilde{Y}_2^* &= \underbrace{Y_{23}+Y_{12}}_{Y_2^*} - \underbrace{\frac{Y_{12}^2}{\Delta Y_{13}+Y_{12}+Y_{13}}}_{e_2^*} \\
\tilde{Y}_3^* &= \underbrace{Y_{13}+Y_{23}}_{Y_3^*} - \underbrace{\frac{Y_{23}^2}{\Delta Y_{12}+Y_{23}+Y_{12}}}_{e_3^*}
\end{aligned} \tag{3.6}$$

where Y_i^* is the measured impedance assuming the zero impedance of shorting path, as inferred from (3.4), e_i^* is the error of the i^{th} measurement compared to ideal case, and Y_{ij} is the accurate connecting impedance.

The difference of the connecting admittance between the ideal and practical cases, $\tilde{Y}_{ij}$, is:

$$\begin{aligned}
\tilde{Y}_{12} - Y_{12} &= 0.5(-e_1^* - e_2^* + e_3^*) \\
\tilde{Y}_{13} - Y_{13} &= 0.5(-e_1^* + e_2^* - e_3^*) \\
\tilde{Y}_{23} - Y_{23} &= 0.5(e_1^* - e_2^* - e_3^*)
\end{aligned} \tag{3.7}$$

This difference depends on the impedance level ratio between ΔY and Y_{ij}. In fact, the shorting path is inductive and its impedance value depends on material and geometry.

In case of high inductive and small capacitive device such as transformers (Liu *et al.*, 1993) or cables (Marlier *et al.*, 2015), the shorting path impedance may be small compared to the connecting impedance at considered frequencies, i.e. $\Delta Y \gg Y_{ij} \longrightarrow e_i^* \approx 0$. Hence, the measured error can be neglected; the impedance matrix is achieved correctly without taking care of the shorting path impedance.

Conversely, the error derived from (3.6) can become significant in this three following cases:

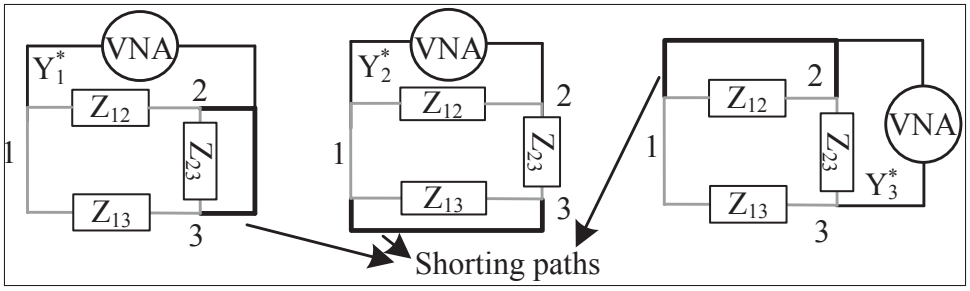


Figure 3.4 Impedance measurement procedure for 3-pin device with perfect shorting impedance paths

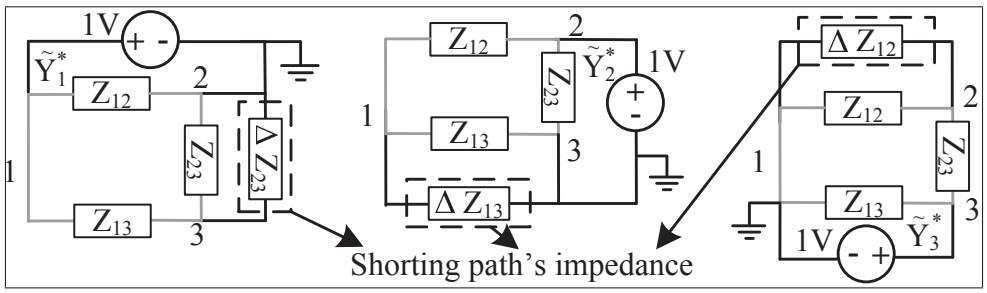


Figure 3.5 Impedance measurement procedure for 3-pin device with imperfect shorting impedance paths

1. If parallel connecting impedance is capacitive at specific frequency range and comparable with that of shorting path impedance, as shown in Fig. 3.6a, e.x. $\Delta Y_{23} \approx -Y_{23} \gg Y_{12}, Y_{13}$, then $e_1^* \approx Y_{13}$, the error can be comparable to connecting admittance. The example for this case is the integrated EMI filter or power supply;

2. In worst case, at any specific frequency range, if $\Delta Y_{23} \approx -(Y_{13} + Y_{23}) \longrightarrow e_1^* \gg Y_{13}^2$, as shown in Fig. 3.6b, the error can be much greater than square of connecting admittance;

3. If the shorting path is poor, i.e. long and thin conductor, its inductance can be in the same order of magnitude to the smallest connecting impedance, as shown in Fig. 3.6c, e.x. $\Delta Y_{23} \approx Y_{13} \gg Y_{12}, Y_{23} \longrightarrow e_1^* \approx Y_{13}/2$, the error can be a half of connecting admittance. An example of this case is the high power transformer with large distance between ports.

In the general case of passive devices with unknown model, no cases can be ignored. For larger pin amount devices, the interaction between shorting paths and connecting impedance becomes

more complicated resulting in unknown measured errors, further degrades the computational precision.

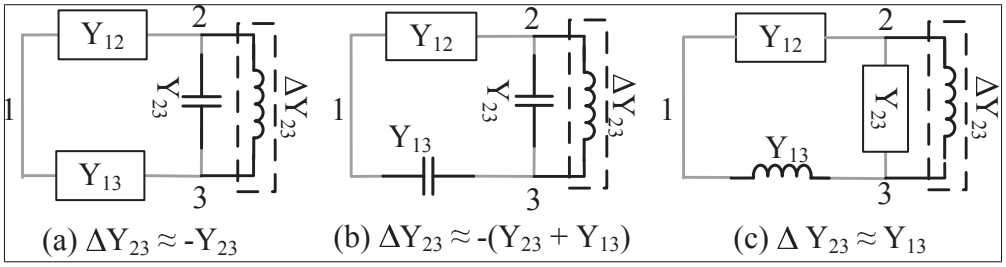


Figure 3.6 Specific cases in which significant errors are created

3.5 Proposed Newton - Raphson method

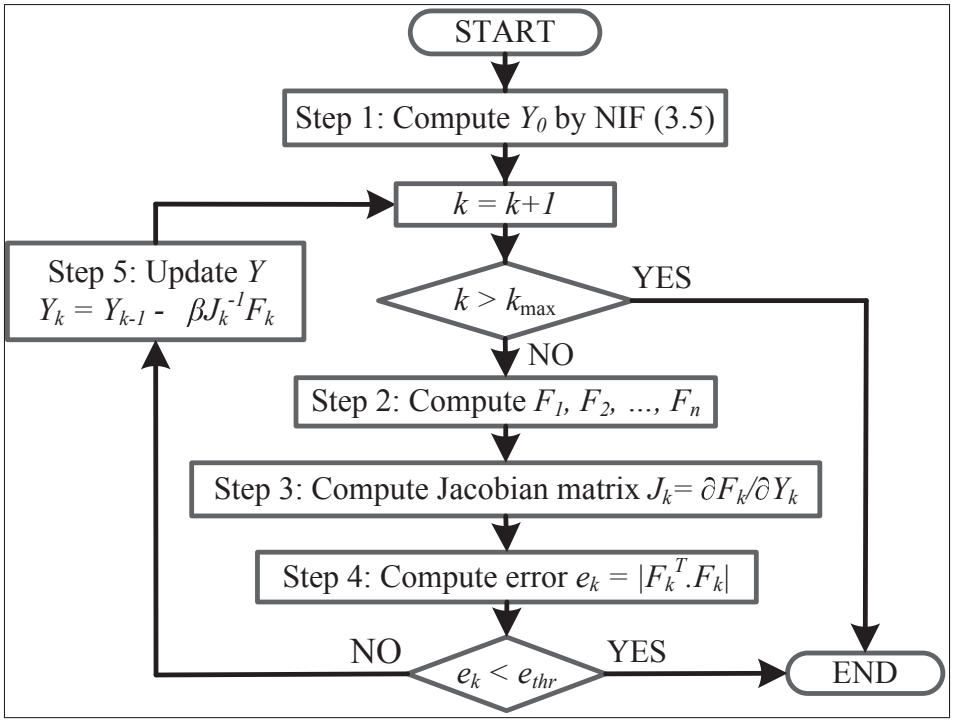


Figure 3.7 Newton-Raphson method for GIR at each frequency

As pointed in the previous section, the precision of NIF model is degraded by the impedance of shorting paths used in measurements. The error level is unknown since it depends on the ratios

between the impedances of shorting paths and the unknown connecting impedance of devices. Therefore, this issue can not be completely solved by only improving the layout of the shorting paths which usually reduces its inductance. Instead, we propose to improve the accuracy of the connecting impedance, which is obtained by the NIF model (3.5) using curve fitting method. To avoid the impact of the impedance of shorting path used in measurements, the fitting curves are chosen as follows:

1. The *open admittance* which is measured by VNA at 2 pins whereas the remaining pins are untouched. Thus, no shorting path appears in measurements;

2. The *VTG* between pin pairs of the devices. A common ground plane is used in measurements, but its influence to the measured data is removed by the S-parameter calibration procedure, as presented in Appendix II. In addition, fitting VTG curves helps to direct the connecting impedance to all correct VTGs between pin pairs of the devices, which is mandatory for computing noise propagation in the power converter via VTGs.

Solving the system of non-linear equations is not obvious without information of the system roots. Thus, we propose to employ the NR iterative method as the fitting algorithm due to its ability of solving non-linear equations for complex variables. The NR method's accuracy and convergence depend on the distance between the *initial guess* and the system roots (Greenspan & Casulli, 1988). Therefore, the connecting impedances obtained by (3.5) are used as the *initial guess* since the gap between them and the system roots is significant only in some specific frequency ranges as discussed in Section. 3.4 and small at the remaining frequency ranges. Instead of these data, an arbitrary *initial guess* can force the NR to diverge or converge to the wrong roots. The summary of proposed NR approach is shown in Fig. 3.7. The details of each step is presented in the next sections.

3.5.1 Step 1: Variables definition

The connecting admittance, Y, is used as the variables for NR iterations. It is initiated by the result obtained in (3.5).

$$\mathbf{Y^0} = [Y_{12}^0, Y_{13}^0, \ \ldots, Y_{(n-1)n}^0]^T = \mathbf{Y}_n \tag{3.8}$$

3.5.2 Step 2: Write NR Functions

The form of NR iteration equations is:

$$\begin{cases} F_1(Y_{12}, Y_{13}, \cdots, Y_{(n-1)n}) = 0 \\ F_2(Y_{12}, Y_{13}, \cdots, Y_{(n-1)n}) = 0 \\ \cdots \quad \cdots \quad \cdots \\ F_{C_n^2}(Y_{12}, Y_{13}, \cdots, Y_{(n-1)n}) = 0 \end{cases} \tag{3.9}$$

Each equation of F_i is formed by equalizing the measured result and their corresponding analytical equations. Two selections of F_i are discussed below with their measurement methods and equation derivations.

3.5.2.1 Open admittance

An example of *open admittance* between pin 1 and pin 2, Y_{12}^{*op}, of a 4-pin device is shown in Fig. 3.8a. Its corresponding closed form equation is derived by considering the VNA as a voltage source. For the sake of generality, this voltage source is excited in both ways: $V_{12} = 1V$ and $V_{21} = 1V$, as depicted in Figs. 3.8b and 3.8c, respectively. The computed *open admittance*

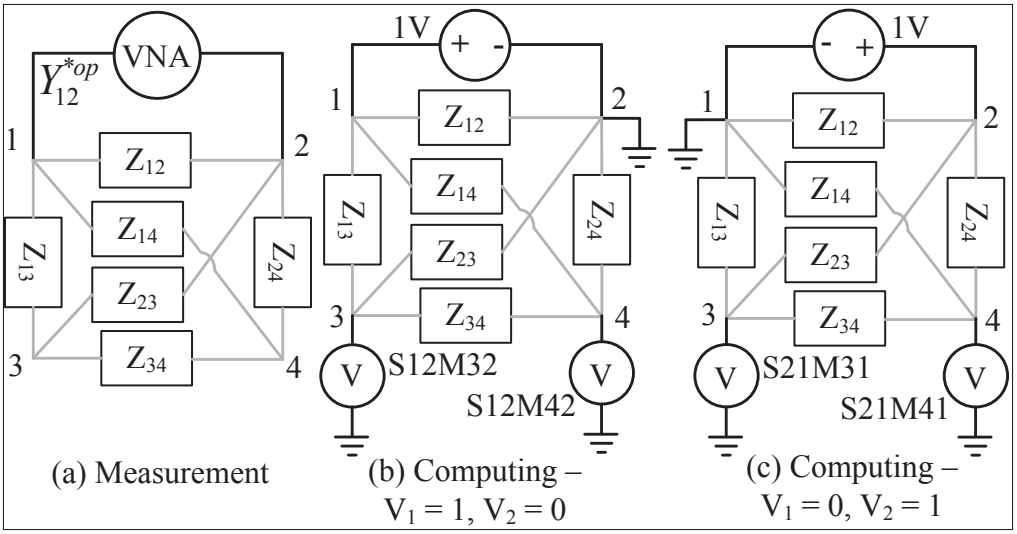


Figure 3.8 Open admittance between pins 1 - 2

is the average of these two sources:

$$Y_{12}^{op} = 0.5 \times \left\{ \sum_{i\neq 1}^{n} Y_{1i} - \begin{bmatrix} Y_{13} & Y_{14} \end{bmatrix} \mathbf{A_{12}}^{-1} \begin{bmatrix} Y_{13} \\ Y_{14} \end{bmatrix} + \sum_{i\neq 2}^{n} Y_{2i} - \begin{bmatrix} Y_{23} & Y_{24} \end{bmatrix} \mathbf{A_{12}}^{-1} \begin{bmatrix} Y_{23} \\ Y_{24} \end{bmatrix} \right\} \tag{3.10}$$

where $\mathbf{A_{12}}$ is defined as the *identified matrix* of pin pair 1-2:

$$\mathbf{A_{12}} = \begin{bmatrix} \sum_{i\neq 3}^{n} Y_{i3} & -Y_{34} \\ -Y_{34} & \sum_{i\neq 4}^{n} Y_{i4} \end{bmatrix} \tag{3.11}$$

In case that the pin number of device increases, i.e. $n - pin$, (3.10) is unchanged. Only $\mathbf{A_{12}}$ is extended to be a $(n-2)\times(n-2)$ matrix. This task is straightforward.

The *open admittance* equation at pins 1-2 for NR is:

$$F_i = Y_{12}^{op} - Y_{12}^{*op} = 0. \tag{3.12}$$

In fact, the NR for a set of all equations of *open admittance* may approach to the wrong root at some specific frequency ranges due to the subtracting operator in (3.10) and the fact that only connecting admittance appears in the equation. During the iterative process, all connecting admittances, Y_{ij}, may reduce to very small amplitudes, resulting in very small amplitudes of both terms $\left\{\sum_{i\neq 1}^{n} Y_{1i} + \sum_{i\neq 2}^{n} Y_{2i}\right\}$ and $\left\{\begin{bmatrix} Y_{13} & Y_{14}\end{bmatrix} \mathbf{A_{12}}^{-1} \begin{bmatrix} Y_{13} \\ Y_{14}\end{bmatrix} + \begin{bmatrix} Y_{23} & Y_{24}\end{bmatrix} \mathbf{A_{12}}^{-1} \begin{bmatrix} Y_{23} \\ Y_{24}\end{bmatrix}\right\}$, while effectively approaching the correct Y_{12}^{op}. As a result, even though the *open admittance* is fit, all the connecting admittances converge to the wrong roots whose amplitudes are very small and presents wrong VTG between pin pairs of devices. This issue is avoided by adding the VTG curve with different form of equation to the system, as presented in the next section.

3.5.2.2 VTGs between pin pairs

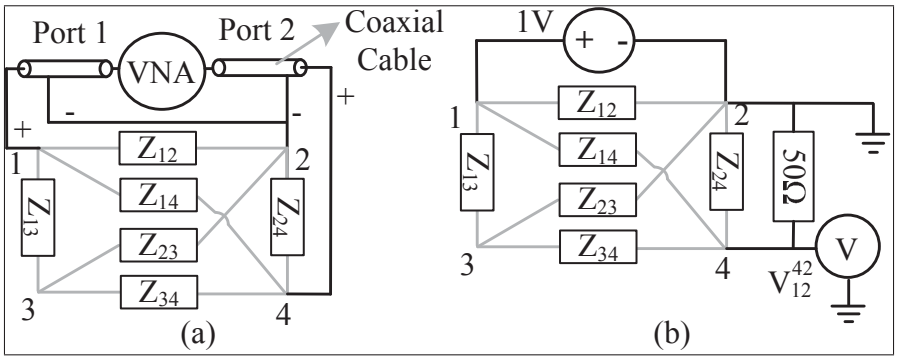


Figure 3.9 VTG (a) Measurement by S- ports (b) Computational model

An example of VTG V_{12}^{42}, where V_{42} is computed/measured considering the excitation source $V_{12} = 1V$, is presented for a 4-pin device. The experimental VTG, V_{12}^{*42}, is obtained indirectly by measuring S- parameters employing coaxial cables, as shown in Fig. 3.9a. The data conversion is introduced in (Pozar, 2009). The analytical equation to compute V_{12}^{42} is derived from

the equivalent circuit shown in Fig. 3.9b as follow.

$$\begin{bmatrix} \cdots \\ V_{12}^{42} \end{bmatrix} = \begin{bmatrix} \sum_{i\neq 3}^{n} Y_{i3} & -Y_{34} \\ -Y_{34} & \sum_{i\neq 4}^{n} Y_{i4} + \dfrac{1}{50} \end{bmatrix}^{-1} \begin{bmatrix} Y_{13} \\ Y_{14} \end{bmatrix} \tag{3.13}$$

where 50Ω is the internal resistor of port 2 of the VNA.

Finally, VTG equation for the NR method is written as:

$$F_i = V_{12}^{42} - V_{12}^{*42} = 0. \tag{3.14}$$

In fact, the VTG below *-80dB* is not used NR equation due to the possible errors created by the precision limit of the VNA.

3.5.2.3 Combined equations

One proposes to use the NR method with the set of equations combined of *open admittance* and VTGs by the procedure described in Fig. 3.10. In which, the GIR is started by the original NIF, and the *open admittance* is used as verification purpose. If the error is not acceptable (condition of "Match measurement" is not satisfied), an equation of VTG is added to improve the computational precision. Otherwise, if the error is very small, the procedure is done, the connecting impedance computed by the original NIF is used as the final result. This is the case of cable and transformer, where errors are negligible as presented in the previous publications (Gustavsen, 2004) - (Marlier *et al.*, 2015).

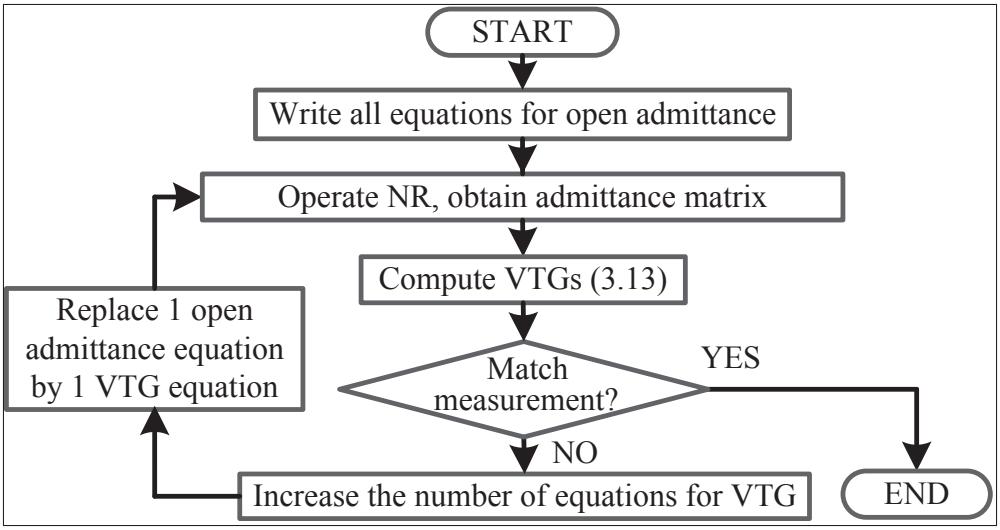


Figure 3.10 Proposed NR with the combined set of equations

3.5.3 Step 3: Jacobian matrix computing

The Jacobian matrix J is the derivative function of F as:

$$\mathbf{J} = \frac{\partial \mathbf{F}}{\partial \mathbf{Y}} = \begin{bmatrix} \frac{\partial F_1}{Y_{12}} & \frac{\partial F_1}{Y_{13}} & \cdots & \frac{\partial F_1}{Y_{(n-1)n}} \\ \frac{\partial F_2}{Y_{12}} & \frac{\partial F_2}{Y_{13}} & \cdots & \frac{\partial F_2}{Y_{(n-1)n}} \\ \vdots & \vdots & \ddots & \vdots \\ \frac{\partial F_{C_n^2}}{Y_{12}} & \frac{\partial F_{C_n^2}}{Y_{13}} & \cdots & \frac{\partial F_{C_n^2}}{Y_{(n-1)n}} \end{bmatrix} \tag{3.15}$$

It must be calculated at each iteration, and usually takes the longest computing time due to the multiple derivative operations. To improve the computation speed, the closed-form function of each element of **J** is derived offline from the closed-form of **F**(3.9) by symbolic mathematical packages. Then, **J** is evaluated at each iteration by placing the real value of variables into its closed - form functions.

3.5.4 Step 4: Error computing

The error at each iteration of NR method is evaluated by:

$$e = \|\mathbf{F}\|^2 = \sum_{i=1}^{n} |F_i|^2 \tag{3.16}$$

The iteration process ends as soon as the error reaches a given threshold, $e < e_{thr}$, where e_{thr} is chosen based on the measurement device precision. For typical devices, whose precision of impedance and VTG is $1m\Omega$ and $-80dB$, respectively, e_{thr} can be chosen at 10^{-8}.

3.5.5 Step 5: Connecting admittance update

The connecting admittance is computed by the generalized Newton's formula (3.17) (Greenspan & Casulli, 1988) - (Kramer & Hitchon, 1997). The o-r factor β is used to control the convergence rate, and hence, must be adjusted carefully to ensure the convergence of the NR method.

$$\mathbf{Y_k} = \mathbf{Y_{k-1}} - \beta \mathbf{J_k}^{-1} \mathbf{F_k} \tag{3.17}$$

3.5.6 Over-relaxation factor computing strategy

Generally, the NR convergence rate is low with too small β but it may diverge with too high β. The selection of β prior to computation is difficult since it depends on the complicated functions of variables, which may vary differently iteration by iteration. To cope with this problem, one proposes an o-r factor computing method to calculate the proper β at each iteration. More precisely, one employs a logic of β control based on the error ratio, which is divided by the errors of current and previous iterations, as shown in Fig. 3.11. This strategy is used between Step 4 and Step 5 of the NR approach.

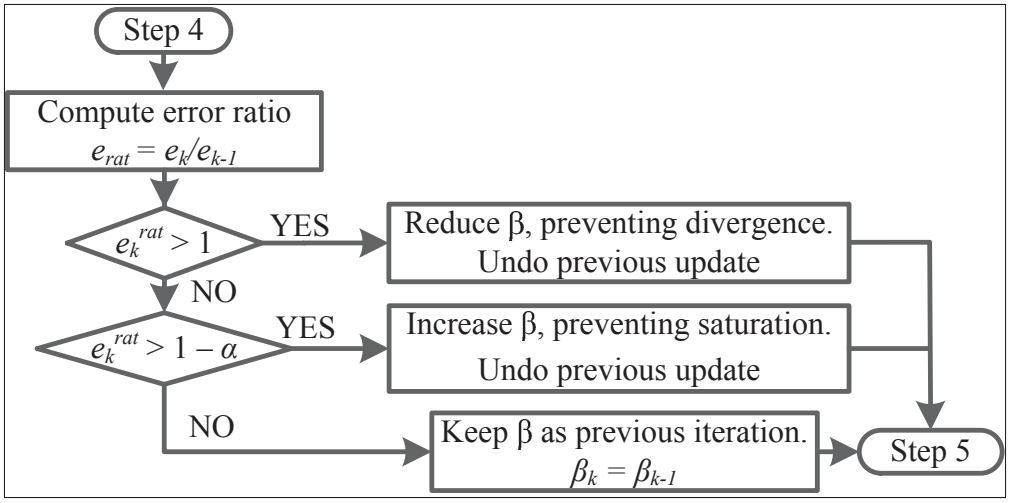


Figure 3.11 Over-relaxation factor computing algorithm

3.6 Experimental results

In this section, the experimental model of an LC filter, formed by the commercial common choke WE-SL2 250μH (L_1) and a 0.1μF capacitor (C_1), is extracted by using GIR. The experimental results present the errors caused by the shorting path impedance regarding to case 1 and case 3 (as discussed in Sec. 3.4), and the effectiveness of the proposed GIR to remove these errors. To remove the impacts of extra components used in measurements, i.e. cables and measured jig's geometry, the measurements are performed in two separate frequency ranges, i.e. 100kHz - 30MHz and 30MHz – 200MHz, with proper calibrations. Considering the LC filter as a 4-pin device, the *initial guess* of the connecting impedance is computed by the impedance measurements taken following the procedure presented in Fig.3.12.

The measured jigs used to extract the impedance and VTG are shown in Fig.3.13. All measurements are performed using a Agilent E5061B VNA. They are presented in Figs.3.14 and 3.15. The following nomenclature is used on these pictures:

- The term "measured" indicates the data extracted by the VNA;
- The term "w/o-NR" indicates the data computed from the connecting impedance obtained in (3.5) without NR (also means the results with the original NIF);

- The term “w-NR” indicates the data computed from the connecting impedance resulted in the NR method (also means the results with GIR.)

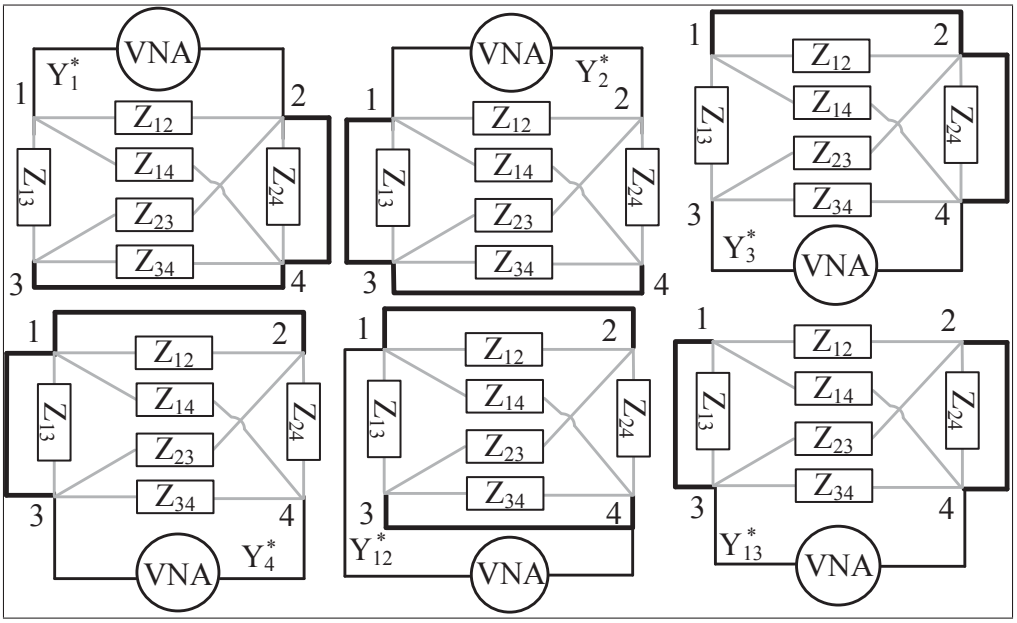


Figure 3.12 Impedance measurement procedure for 4-pin device

3.6.1 Experimental results at conducted EMI frequencies

The experimental results of the LC filter in frequency range 100kHz – 30MHz is shown in Fig. 3.14. Fig. 3.14a shows 6 measured group - impedance described in Fig. 3.3. One observes the small impedance of Z_3^*, Z_4^*, Z_{13}^* and Z_{14}^* in frequency range 3–7MHz.They are used in (3.5) to compute the connecting impedances, i.e. Z_{ij}w/o-NR, also used as the *initial guess* of NR, as introduced in Sec. 3.5.1.

The impact of the shorting path impedance is shown in Fig. 3.14b by the differences between computation w/o-NR and measurements of V_{12}^{32}, V_{12}^{42}, Z_{12}^{op} and Z_{34}^{op} in frequency range 3–7MHz. These differences are caused by the interaction between the small impedance of C_1 and the impedance of shorting paths as given in Fig. 3.6b, and analyzed in Sec. 3.4.Similar disturbances are observed in the performances of VTGs V_{14}^{34}, V_{24}^{34} and V_{13}^{23} as shown in Fig. 3.14d.

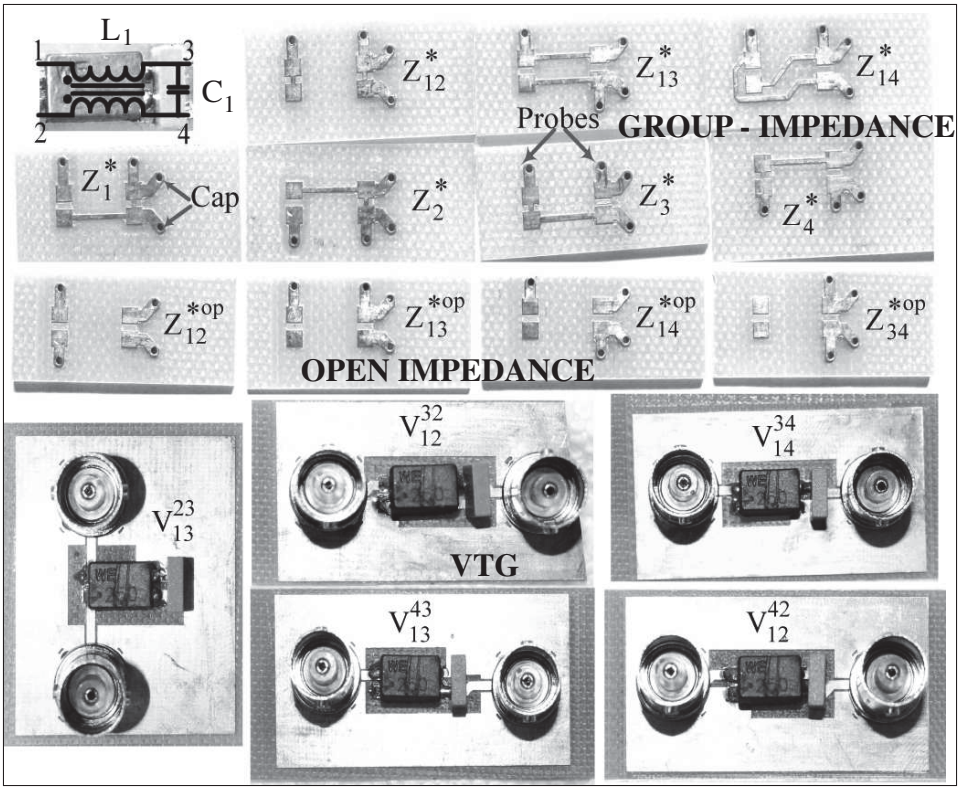


Figure 3.13 Measured prototypes of the LC filter

To eliminate these errors, the proposed NR method is employed. As the symmetry of L_1, i.e. $Z_{13} = Z_{24}$ and $Z_{14} = Z_{23}$, instead of 6 equations for the general case, only 4 equations are needed to solve the 4 connecting impedance variables. The equations of V_{12}^{32}, V_{12}^{42}, Z_{12}^{op} and Z_{34}^{op} are written as described in Sec.3.5.2. Thanks to the proposed NR method, V_{12}^{32}, V_{12}^{42}, Z_{12}^{op} and Z_{34}^{op} fit well with measurements, as observed in Fig. 3.14b.

The curves of connecting impedance obtained by GIR with and without NR method are shown in Fig. 3.14c. One observes the significant improvements of the connecting impedance Z_{13} and Z_{14} in frequency range 3–7MHz. The same improvement is observed on Z_{34} in frequency range 3–30MHz whereas Z_{12} remains unchanged. The small changes of all connecting impedance below 1 MHz are to fit the VTG V_{12}^{42}. They correspond well to the disturbances as aforementioned.

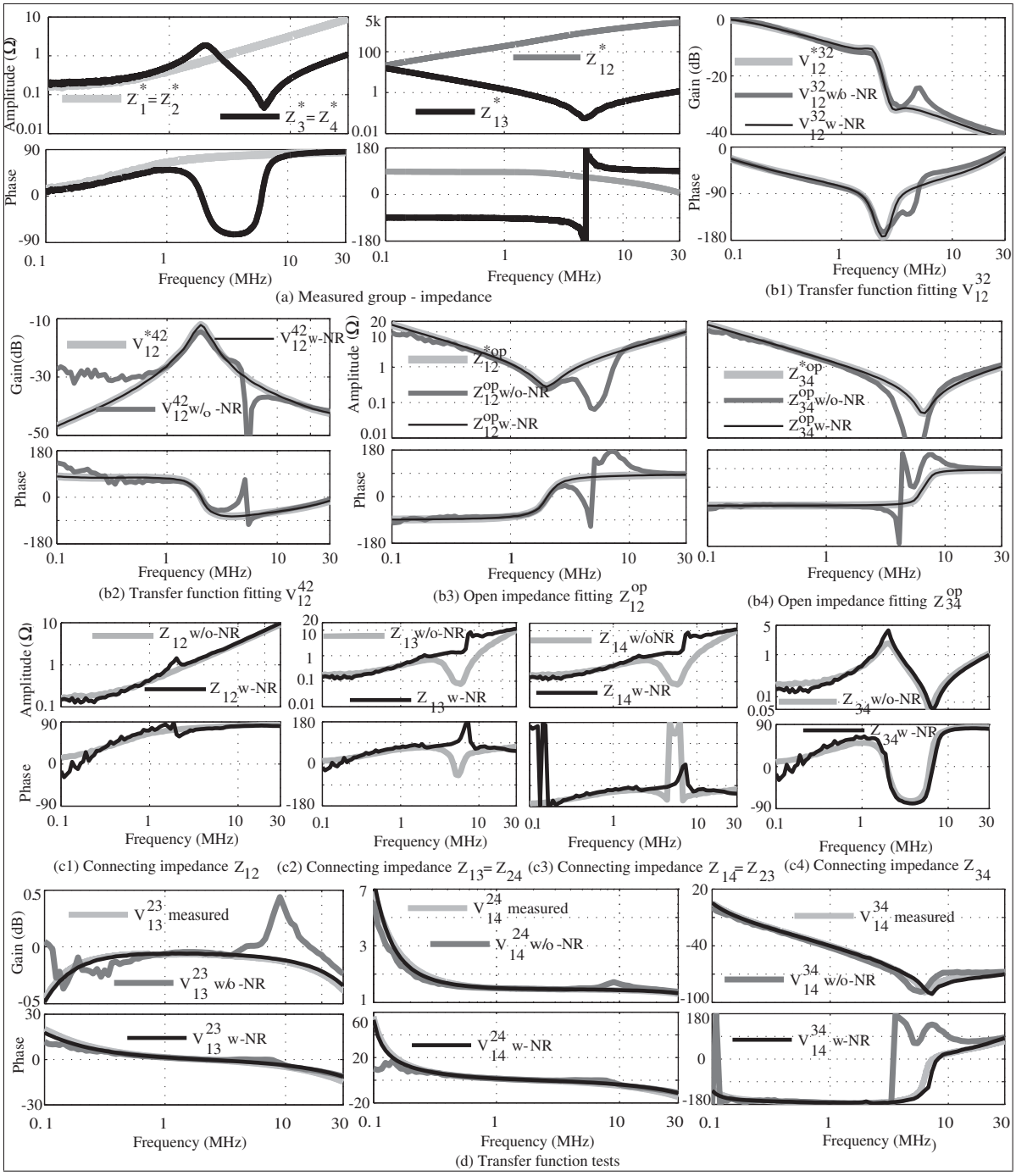


Figure 3.14 Experimental results for LC filter at low frequency

The VTGs V_{14}^{34}, V_{24}^{34} and V_{13}^{23}, not used to be fit by NR, are plotted in Fig. 3.14d. As observed, the VTGs obtained by NR overlap their measurements well including small gains of V_{14}^{34} and

V_{24}^{34} as well as nearly unity gain of V_{13}^{23}. The small error appearing on V_{24}^{34} at frequency of 2MHz results from small errors in measurements at the corner frequency of Z_{12}^{*op}, V_{12}^{*32} and V_{12}^{*42}.

3.6.2 Experimental results at radiated EMI frequencies

This section presents the experimental results of the LC filter in frequency range 30MHz – 200MHz, shown in Fig. 3.15, to point out the effectiveness of NR to correct the errors caused as case 3 introduced in Sec. 3.4. Fig. 3.15a shows the measured group - impedance. It is observed that the inductive behaviors of $Z_1^* = Z_2^*$ and $Z_3^* = Z_4^*$ decreases with frequency. The *initial guess* of NR is computed from these data as mentioned in Sec. 3.6.1.

The effect of shorting path impedance is shown in Fig. 3.15b by the gap between measurement and computation of V_{12}^{32}, V_{12}^{42}, Z_{12}^{op} and Z_{34}^{op}. The differences between measurements and computations are small with the biggest errors of 4dB of V_{12}^{32}, shown in Fig. 3.15b1. One also observes that the error magnitude increases with frequency for all data. This error increasing is caused by the impedance of the shorting path (PCB trace which is mostly inductive) increases faster than connecting impedance (whose inductance usually reduces with frequency), leading to higher error at high frequency. This is the error case 3 discussed in Sec. 3.4. This trend is confirmed with the disturbances of V_{13}^{43} and V_{34}^{14}, shown in Fig. 3.15d.

In order to remove these errors, the proposed NR approach is used to fit the computations with measurements of V_{12}^{32}, V_{12}^{42}, Z_{12}^{op} and Z_{34}^{op}. It results in the connecting impedance shown in Fig. 3.15c. One observes the significant improvements of the connecting impedance, i.e. Z_{12} and Z_{34} in frequency of 80MHz - 200MHz; Z_{13} and Z_{14} in frequency of 30MHz - 200MHz, thanks to proposed NR method. It shows that the inductance of common choke decreases with frequency, which is a typical behavior. The accuracy of the proposed method is validated by the performances of VTGs V_{13}^{23}, V_{13}^{43} and V_{34}^{14}, depicted in Fig. 3.15e. As seen, the VTGs computed from connecting impedance obtained by NR match their measurement very well. It is a very good improvement considering the errors of 20dB (V_{13}^{43}) and 10dB (V_{34}^{14}) achieved with the original connecting impedance computed by the original NIF.

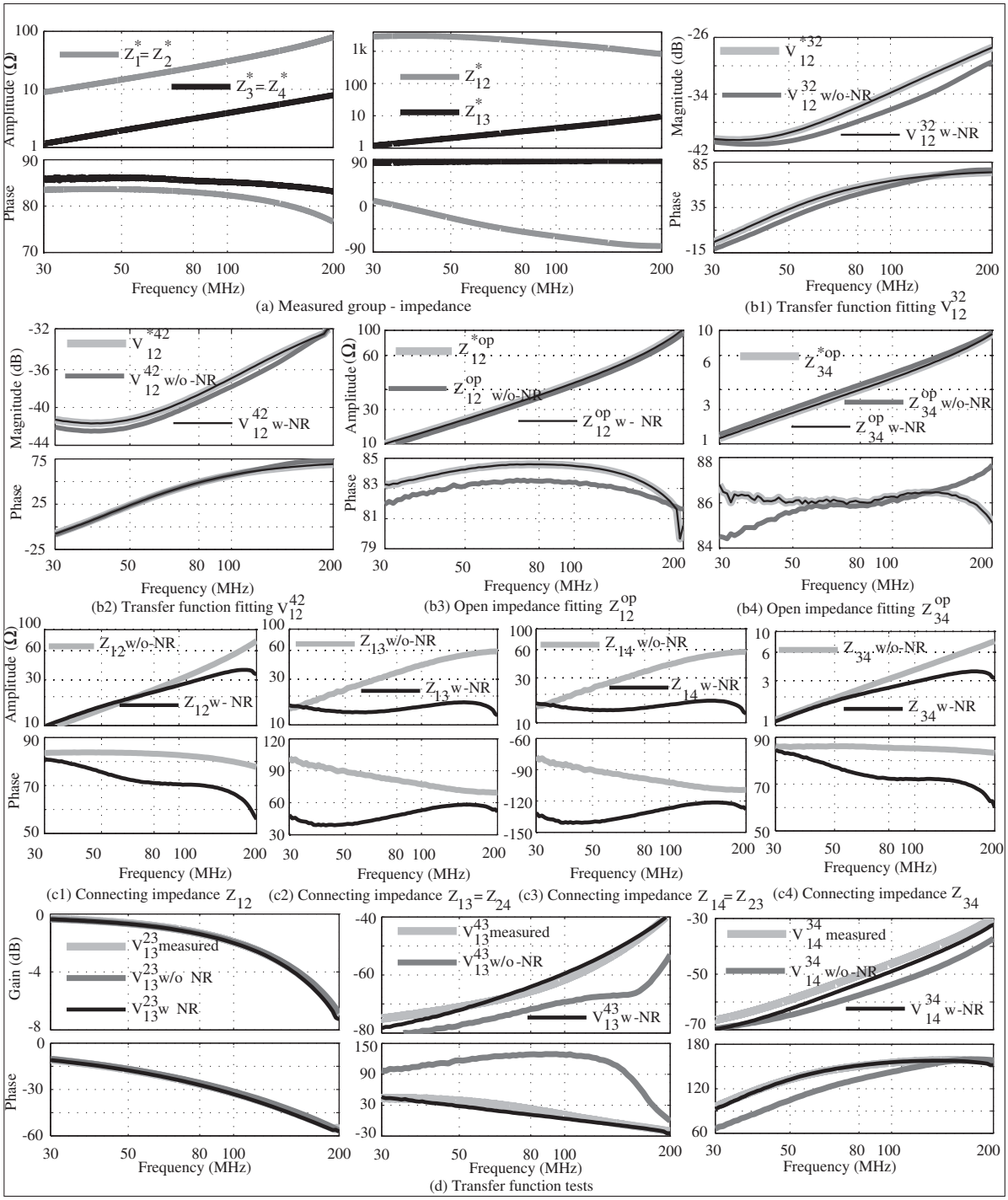


Figure 3.15 Experimental results for LC filter at high frequency

The characteristics of NR method are illustrated in Fig. 3.16 including error, o-r factor and number of iterations. As seen, the o-r factor is 0.4 and only few iterations are needed in

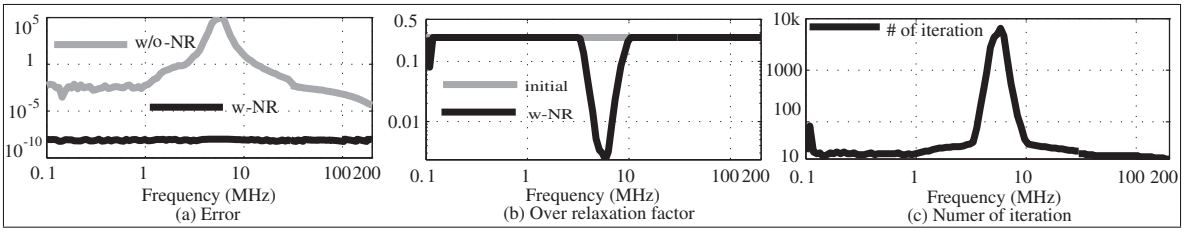


Figure 3.16 Newton Raphson characteristics

frequency below 1MHz and above 30MHz since the *initial guess* is very close to the root, shown by small errors in those frequency ranges. In addition, the lowest o-r factor and highest number of iterations correspond to the highest initial error in the frequency of 3–30MHz. For instance, the o-r factor is decreased to prevent NR from diverging making the convergence rate slower than that in the remaining frequency ranges. It confirms the effectiveness of computing approach proposed in Sec.3.5.6. In addition, Fig. 3.16a also shows that the proposed GIR is dedicated to correct both small errors, usually present with cables and transformer using NIF, and significant errors, where NIF is not accurate to implement.

3.7 Conclusion

In this chapter, an effective GIR is proposed for modeling the passive device used in power converter based on the measurements of impedance and Scattering parameters. It is developed from the original NIF with the improvement of correcting computational errors created by the shorting path impedance used in the measurement procedure. This chapter also introduces the new measured data, i.e. VTG and *open impedance*, and the complete identification procedure required to ensure the model accuracy. In addition, the computing approach for over-relaxation method is proposed to the NR convergence with different input data. As a result, the proposed GIR is precise whether the effect on the shorting path impedance is negligible (as NIF), or significant (as the considered components in this chapter). Thanks to GIR, all passive devices without specific models can be accurately modeled and integrated into the power converter EMI model to predict the noise spectrum of the next generation of SiCFET and GaN - based converter.

CHAPTER 4

AN ACCURATE MODELING APPROACH TO COMPUTE NOISE TRANSFER GAIN IN COMPLEX LOW POWER RAILS GEOMETRIES OF POWER CONVERTERS

4.1 Motivation and Summary

Motivation

In power converter, all functional circuits in the low power circuit, i.e. gate driver, current/voltage sensing and micro-controller, are supplied by a common supply rails, as shown in Fig. 4.1. Since it is the link between the noise sources (gate drivers) and several functional circuits, the low power rails has an essential role on controlling noise propagation in the low power circuit. As pointed in Section 2.3.2, the impedance of the low power rail seen from the gate driver has strong influence on current spectra in the low power circuit. Therefore, this impedance must be controlled to ensure the low noise current in the low power circuit. However, the complexity of this impedance increases with the number of devices and circuits in the low power circuit. Especially, with recently developed multi-port converters (Wu *et al.*, 2015) and modular multilevel converters (Hagiwara & Akagi, 2009), the low power rail design becomes more critical for supplying the numerous devices attached to it.

There are two ways to design the low power rail depending on the applications.

In laboratory research, one can use a high cost commercial DC source to supply the low power rail, connecting to the Gate driver and controller circuit by wires, as shown in Fig. 4.2. In this case, the low power rail impedance depends on impedance of the power supply, which is unknown, and the wires connecting power supply with the functional circuits, which can be complicated by the transmission line effect due to its length. Therefore, the designers have no control on the noise propagation in the low power circuit, resulting in poor converter reliability.

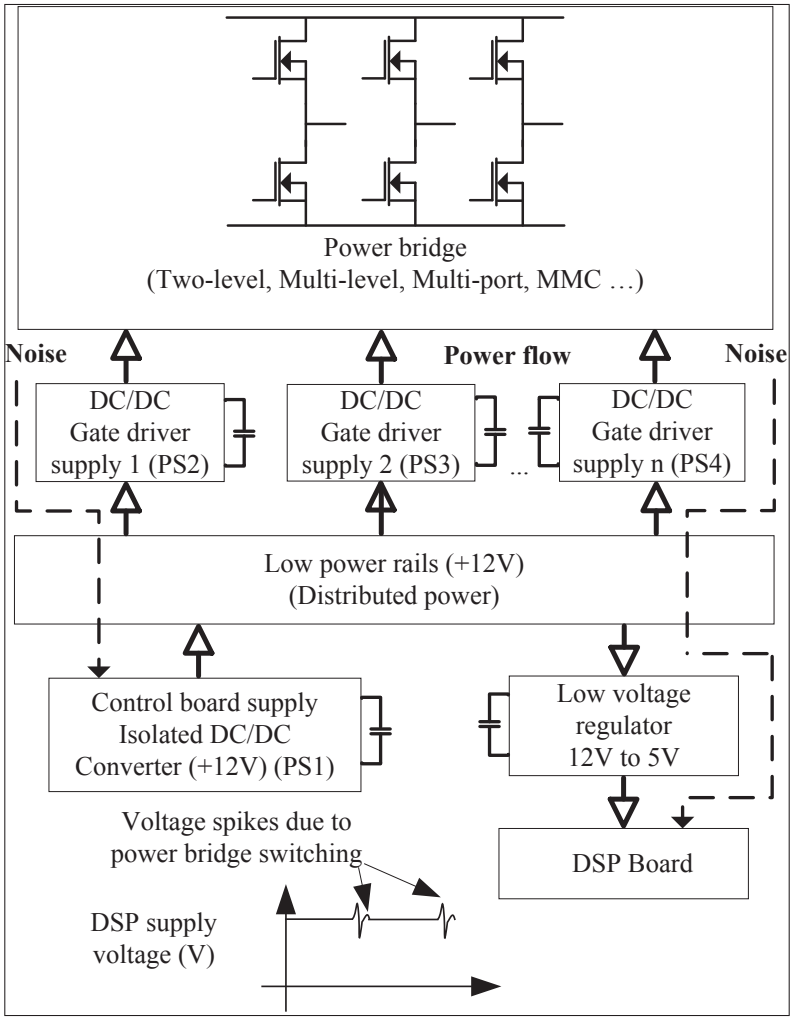


Figure 4.1 Noise propagation in low power circuit of converter

Conversely, in industry, to ensure the low cost product with high density, production ability and high reliability, all parts of the converter must be placed compactly together. In this case, the low power rail is designed as the power/ground structure in PCB to achieve low impedance, as given in Fig.4.3. However, it is not trivial to control the impedance of the low power rail for low noise profile purpose due to three following reasons. First, the low power rail geometry is complex due to its dependency on locations of functional circuits and clearance constraints in the PCB giving difficulty to control its impedance, specifically in EMI frequency range. Second, what is the equivalent impedance of the complete low power rail which is the combination of impedance of functional circuits and that of the low power rail PCB taken into account the

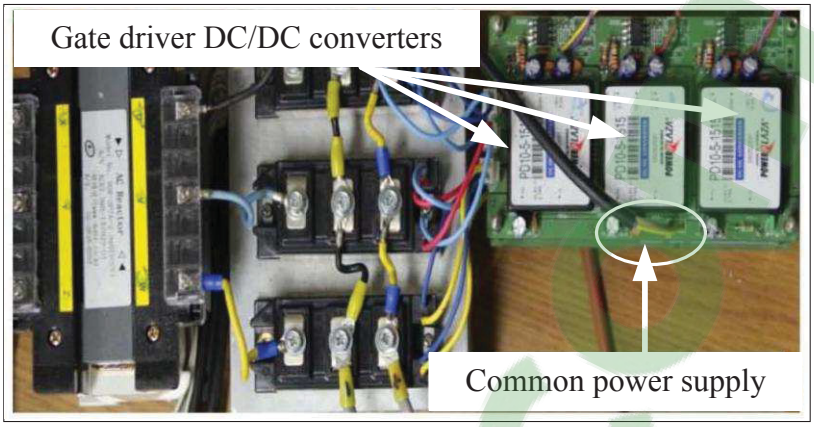


Figure 4.2 Supply for Gate driver of a laboratory prototype
Taken from Nguyen (2012)

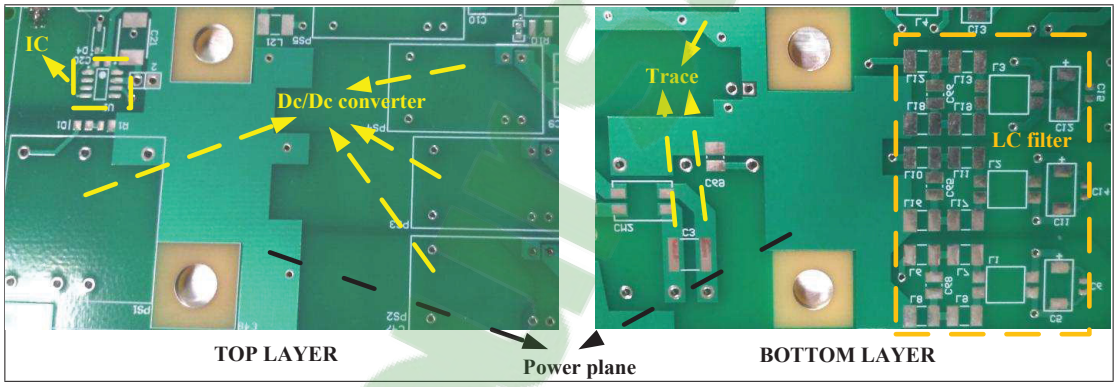


Figure 4.3 Low power rails of a power converter used in industrial application

locations of functional circuits and complex geometry PCB? Third, the low power rail is connected to functional circuits at multiple connecting points, hence, how can impedance seen from one point to the other point affect on noise propagation? These above questions are the motivation to develop a new modeling technique for low power rail, which will be proposed in this chapter.

Summary

In this chapter, we propose a modeling approach based on 2D lumped model to quantify voltage transfer gain (VTG) between each port pair in low power rail and analyze the effect of EMI attenuators on VTG. The advantage of the modeling approach is the ease with which usual noise

reduction devices such as decoupling capacitors or ferrite beads can be integrated in the model. This feature is enforced by a new modular approach based on effective matrix partitioning, which is presented in the chapter. This partitioning is used to decouple power rails equations from external device impedance, thereby avoiding rewriting of the whole set of equation at every change. In addition, the current boundary conditions are utilized to deal with the complex geometry of the low power rails without extra computation. The model is quickly solved in frequency domain, which is well suited for an automated layout optimization algorithm. Using frequency domain modeling also allows the integration of frequency-dependent devices such inductors and capacitors which are required for realistic computation results. Based on the VTG results, the effect of each external device on VTG is analyzed in detail, providing insight into the optimal design of EMI attenuation. In order to check the precision of the modeling approach, VTG for several layout configurations is computed and compared with experimental measurements based on scattering parameters. The contents of this chapter was published in *Journal of Power Electronics*, in March 2017 (Nguyen *et al.*, 2017c).

4.2 Power/ground plane modeling

In recent years, power/ground plane structures have been widely investigated by microwave researchers. The rectangular power/ground plane, which features the simplest geometry, has been efficiently modeled by the cavity - lumped model (Lei *et al.*, 1999; Hampe & Dickmann, 2005; Fan *et al.*, 2001). The decoupling capacitor is taken into account by the transmission line elements method (Kim *et al.*, 2004; Guo & Hubing, 2006; Hampe *et al.*, 2007). The above approaches are fast and accurate but unable to analyze the power/ground plane in complex geometry which is typical in power electronic board designs.

Several approaches have been developed for irregular power/ground plane geometries. The 2D contour integral equation method is introduced in (Štumpf & Leone, 2009; Štumpf, 2014), which separates the arbitrary shape into small segments with an assumption of uniformly distributed voltage. A FEM - SPICE method (Smith *et al.*, 2001; Bednarz *et al.*, 2014) requires heavy computation for complex PCB structure. The arbitrary power/ground plane is model is

time-domain by discontinuous Galerkin method (Lee *et al.*, 2015). A multi-conductor transmission line based on lumped model is presented in (Sourajeet & Dounavis, 2013; Kim & Swaminathan, 2001). This method represents the irregular geometry by the combination of rectangular cells in order to apply the established lumped model for rectangular shape of the PCB. As the geometry complexity increases, the segmentation, and hence, the full model becomes more complicated. (Kim & Swaminathan, 2001) takes the decoupling capacitor into account as a multiplied matrix, where its impedance is placed on diagonal line with assumption of the device's small dimensions. It prevents the approach from modeling large dimension devices which are usually placed in the power/ground plane. In addition, optimization for decoupling capacitor selection and placement is difficult since its matrix interacts with the whole set of equation.

4.3 Modeling approach

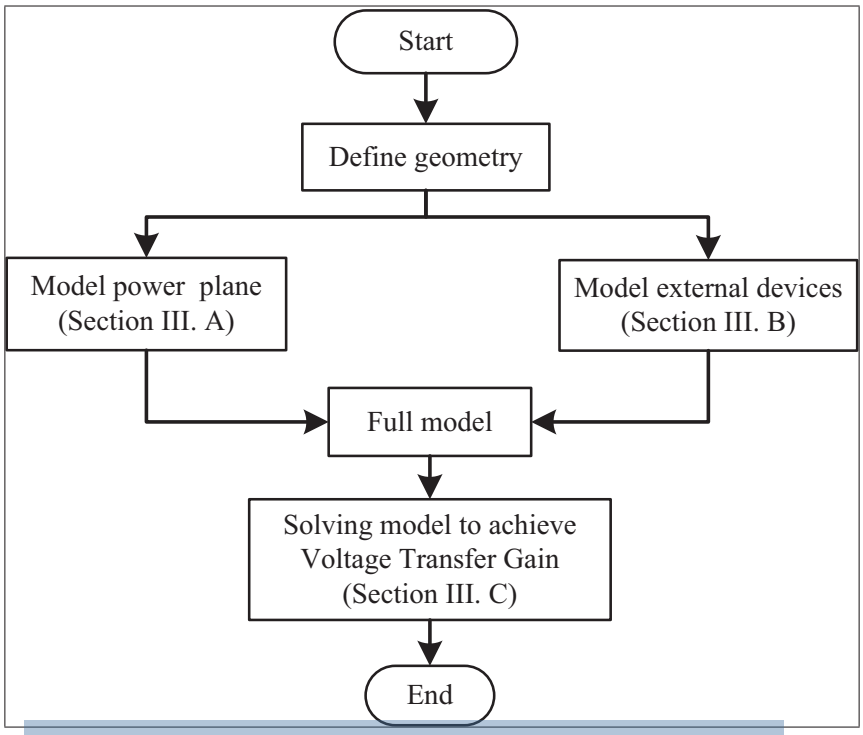


Figure 4.4 Modeling approach

The approach is developed to obtain the full model of the low-power rails with all external devices placed on it. The main idea of this approach is to model low power rails and the external devices separately, as summarized in Fig. 4.4.

First, the low power rails geometry is separated into a number of small parts (herein called '*cell*') with dimensions $dx \times dy$. Based on several numerical investigations, cell dimensions 10 times smaller than the signal wavelength must be chosen, to guarantee constant current and voltage over the cell. Without losing generality, the power rails is assumed to be separated into n cells through the rest of this chapter. Second, the power rails and the external devices are modeled independently before combining into the full model. Considering the fact that these parasitic components may be different from those introduced in the datasheet, we suggest experimentally measuring the impedance of external devices to guarantee the accuracy of computational results. Third, the model is solved to obtain both the voltage distribution and VTG. These steps will be introduced in details in the next sections.

4.3.1 2D Lumped model for complex low power rails geometry

The 2D lumped model is used to model each cell of low power rails (Kim & Swaminathan, 2001).

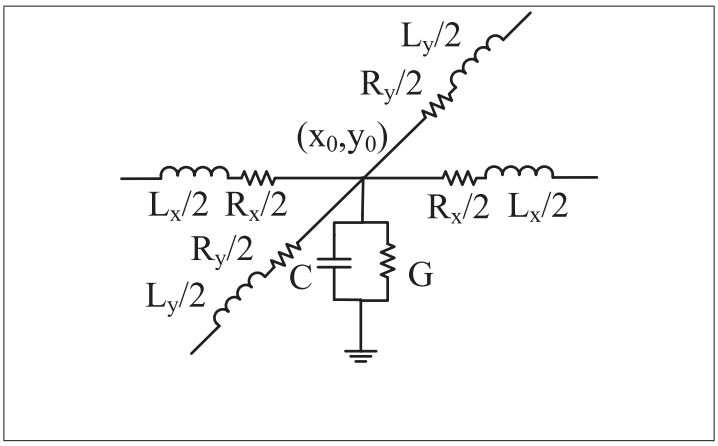


Figure 4.5 Lumped model of one cell

As shown in Fig. 4.5, each cell is connected to 4 surrounding cells by serial resistances (R_x, R_y) and serial inductance (L_x, L_y). In addition, impedance between power and ground planes is represented by a shunt conductance (G) and a shunt capacitance (C). In the events that parts of the low power rails have a small dimension, the cell parameters can be extracted using the finite element method. On the other hand, if the conduction width is very large, compared to the PCB thickness, the border effect can be neglected resulting in uniform field distribution between the planes. In such a case, the parallel plane approximation is valid and cell parameters are computed by the following equations (Pozar, 2009).

$$\begin{aligned} L_x &= \frac{\mu h dx}{dy}; & L_y &= \frac{\mu h dy}{dx} \\ R_x &= \frac{2R_s dx}{dy}; & R_y &= \frac{2R_s dy}{dx} \\ C &= \frac{\varepsilon dx dy}{h}; & G &= \omega \delta C \end{aligned} \tag{4.1}$$

where ω is the considered frequency, h is the height of dielectric, μ is permeability, δ is loss tangent, ε is permittivity and R_s is surface resistivity of the material.

To obtain voltage and current distributions over the plane, the Kirchhoff equations are developed in the remaining part of this section. In order to keep things simple, the closed form equations are presented for a simple plane, making extension to complex plane geometry is straightforward.

Fig. 4.6 shows a typical L-shape geometry low power rails discretized into 10 cells corresponding to node voltage ($\mathbf{V}(1)$, $\mathbf{V}(2)$... $\mathbf{V}(10)$.) Of course, Kirchhoff's equations must be applied to all cells, but due to the limited space, only equations for cell number 6 are presented. Current and voltage definition of cell 6 are shown in Fig. 4.7. Applying Kirchhoff's voltage law in $x-$

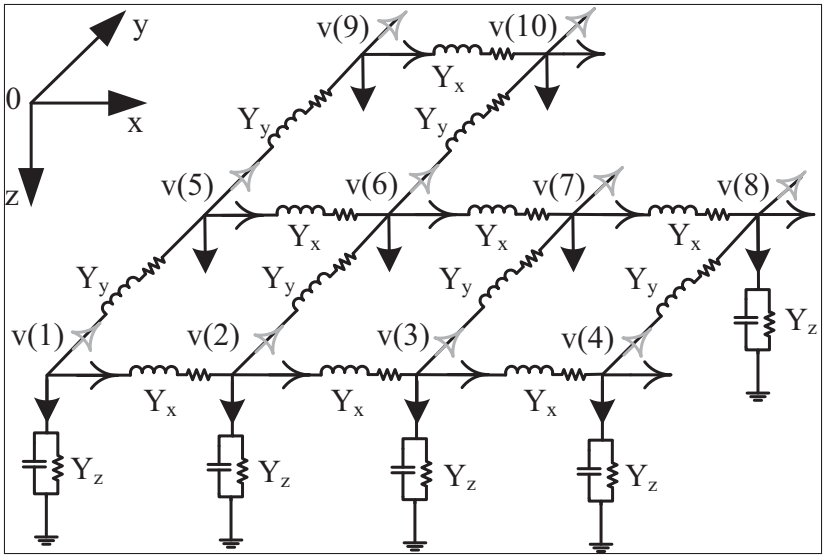


Figure 4.6 Example for a 2D model of power rails

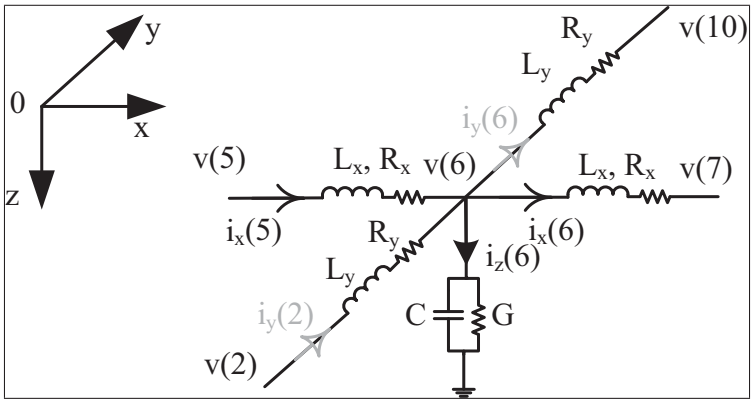


Figure 4.7 Voltage and current definition at cell 6

and $y-$ directions yields (4.2) and (4.3), respectively:

$$i_x(6) = [v(6) - v(7)]\,(R_x + j\omega L_x)^{-1} \tag{4.2}$$

$$i_y(6) = [v(6) - v(10)]\,(R_y + j\omega L_y)^{-1} \tag{4.3}$$

The Kirchhoff's current law yields:

$$\begin{aligned} i_z(6) &= v(6)\left(G+\frac{1}{j\omega C}\right)^{-1} \\ &= i_x(5)-i_x(6)+i_y(2)-i_y(6) \end{aligned} \tag{4.4}$$

The current of each cell is linked to that of the *neighbor cell*. Cell m is defined as $x-neighbor$ or $y-neighbor$ of cell k if (4.5) or (4.6) is satisfied, respectively.

$$\begin{cases} \mathbf{X}(m)-\mathbf{X}(k) &= dx \\ \mathbf{Y}(m)-\mathbf{Y}(k) &= 0 \end{cases} \tag{4.5}$$

$$\begin{cases} \mathbf{X}(m)-\mathbf{X}(k) &= 0 \\ \mathbf{Y}(m)-\mathbf{Y}(k) &= dy \end{cases} \tag{4.6}$$

Vectors $\mathbf{Q_x}$ and $\mathbf{Q_y}$ are defined as $x-neighbor$ and $y-neighbor$ vectors, respectively.

$$\mathbf{Q_x}(k) = \begin{cases} m & \text{if} \quad \exists m \text{ satisfies (4.5)} \\ 0 \text{ if} & \nexists m \text{ satisfies (4.5)} \end{cases} \tag{4.7}$$

$$\mathbf{Q_y}(k) = \begin{cases} m & \text{if} \quad \exists m \text{ satisfies (4.6)} \\ 0 \text{ if} & \nexists m \text{ satisfies (4.6)} \end{cases} \tag{4.8}$$

For instance, in Fig. 4.6, these vectors are:

$\mathbf{Q_x} = [2\ 3\ 4\ 0\ 6\ 7\ 8\ 0\ 10\ 0]^T$, $\mathbf{Q_y} = [5\ 6\ 7\ 8\ 9\ 10\ 0\ 0\ 0\ 0]^T$. Obviously, the currents flowing outside the low power rails must be zero. This condition is applied to a cell that doesn't have x or $y-neighbor$ using the definitions of $\mathbf{Q_x}$ and $\mathbf{Q_y}$:

$$i_x(k) = 0 \quad \text{only if} \quad \mathbf{Q_x}(k) = 0 \tag{4.9}$$

$$i_y(k) = 0 \quad \text{only if} \quad \mathbf{Q_y}(k) = 0 \tag{4.10}$$

As clearly shown in (4.9) and (4.10), forcing $i_x(k)$ and/or $i_y(k)$ to zero can define the border cells represented by $\mathbf{Q_x}$ and $\mathbf{Q_y}$, and then, the geometry of low power rails. This is the current boundary condition to tackle the irregular geometry of low power rails as long as cells are either rectangular or approximated as a rectangular shape. This condition is generally met for PCB design in power electronic applications. In the example shown in Fig. 4.6, the current boundary conditions written as:

$$i_x(4) = i_x(8) = i_x(10) = 0 \tag{4.11}$$

$$i_y(7) = i_y(8) = i_y(9) = i_y(10) = 0 \tag{4.12}$$

In a more general way, based on cell equations (4.2)-(4.4) and the above definitions (4.5)-(4.10), the general Kirchhoff's law for the cells shown in Fig. 4.6 are written in the matrix form as:

$$\mathbf{I_x} = \mathbf{Y_x A V} \tag{4.13}$$

$$\mathbf{I_y} = \mathbf{Y_y B V} \tag{4.14}$$

$$\mathbf{E I_x} + \mathbf{D I_y} = \mathbf{Y_z V} \tag{4.15}$$

where $\mathbf{V}$, $\mathbf{I_x}$ and $\mathbf{I_y}$ are $n \times 1$ column vectors representing voltages and currents in $x-$ and $y-$ directions of all cells respectively. $\mathbf{Y_x}$, $\mathbf{Y_y}$ and $\mathbf{Y_z}$ are $n \times n$ diagonal admittance matrices in $x-$, $y-$ and $z-$ direction, respectively. (4.13) and (4.14) are the Kirchhoff's voltage law equations in $x-$ and $y-$ directions, respectively. (4.15) is the Kirchhoff's current law equation at each cell. The admittance matrices are described as follows.

$$\mathbf{Y_x}(p,p) = [\mathbf{R_x}(p) + j\omega \mathbf{L_x}(p)]^{-1} \tag{4.16}$$

$$\mathbf{Y_y}(p,p) = [\mathbf{R_y}(p) + j\omega \mathbf{L_y}(p)]^{-1} \tag{4.17}$$

$$\mathbf{Y_z}(p,p) = \left[\mathbf{G}(p) + \frac{1}{j\omega \mathbf{C}(p)}\right]^{-1} \tag{4.18}$$

where p stands for the cell's number. **A**, **B**, **D** and **E** are $n \times n$ transformation matrices which are given as follows.

$$\mathbf{A}(p,q) = \begin{cases} 1 & \text{if} \quad q = p & \text{and} \quad \mathbf{Q_x}(p) \neq 0 \\ -1 & \text{if} \quad q = \mathbf{Q_x}(p) & \text{and} \quad \mathbf{Q_x}(p) \neq 0 \\ 0 & \text{otherwise.} \end{cases} \tag{4.19}$$

$$\mathbf{B}(p,q) = \begin{cases} 1 & \text{if} \quad q = p & \text{and} \quad \mathbf{Q_y}(p) \neq 0 \\ -1 & \text{if} \quad q = \mathbf{Q_y}(p) & \text{and} \quad \mathbf{Q_y}(p) \neq 0 \\ 0 & \text{otherwise.} \end{cases} \tag{4.20}$$

$$\mathbf{E}(p,q) = \begin{cases} -1 & \text{if} \quad q = p & \text{and} \quad \mathbf{Q_x}(p) \neq 0 \\ 1 & \text{if} \quad p = \mathbf{Q_x}(q) & \text{and} \quad \mathbf{Q_x}(p) \neq 0 \\ 0 & \text{otherwise.} \end{cases} \tag{4.21}$$

$$\mathbf{D}(p,q) = \begin{cases} -1 & \text{if} \quad q = p & \text{and} \quad \mathbf{Q_y}(p) \neq 0 \\ 1 & \text{if} \quad p = \mathbf{Q_y}(q) & \text{and} \quad \mathbf{Q_y}(p) \neq 0 \\ 0 & \text{otherwise.} \end{cases} \tag{4.22}$$

In (4.19)-(4.22), conditions $\mathbf{Q_x}(p) \neq 0$ and $\mathbf{Q_y}(p) \neq 0$ are utilized to impose current boundary conditions (4.9) - (4.10).

4.3.2 External device modeling

In this section, models of typical devices powered by a low power rails such as DC/DC converters, decoupling capacitors or filters, are presented. In practice, external devices are soldered to PCB through pads and vias which can affect on noise performance. However, the effect of vias can be negligible due to their low impedance below 100MHz. Moreover, the coupling between low power rails and external devices are also neglected in EMI frequency range. The modeling of this part involves the following two steps.

1. The impedance of devices is measured experimentally using the Network Analyzer. It ensures the accuracy of parasitic elements of the device which may vary unexpectedly

from manufacturer specifications. The impedance is measured by scattering parameters with the proper methods, i.e. series and shunt thru, due to the impedance level in each frequency range;

2. The auxiliary admittance matrix $\mathbf{Y_{aux}}$ is created by inserting the impedance of devices at the matrix's positions corresponding to the devices' physical locations. There are two locations of equivalent impedance in $\mathbf{Y_{aux}}$ according to the device's physical dimensions. In a case where the device's dimensions are smaller than cell's dimensions, as a decoupling capacitor, the equivalent impedance is placed in the diagonal line at the cell's number. Otherwise, once the device's dimensions are larger than cell's dimensions, as with a DC/DC converter, the equivalent impedance is placed at positions where column and row correspond to the cell's number to which the device is attached. Generally, $\mathbf{Y_{aux}}$ is defined as follow.

$$\mathbf{Y_{aux}}(p,q) = \begin{cases} Z_{pq}^{-1} & \text{if } \exists Z_{pq} \text{ at cells } p \text{ - } q \\ 0 & \text{otherwise.} \end{cases} \tag{4.23}$$

Then, the full admittance between power and ground is obtained as $\mathbf{Y_{aux}} + \mathbf{Y_z}$. Using $\mathbf{Y_{aux}}$ as an additional matrix provides several advantages.

First, it is easy to change/add new devices in the model by simply modifying $\mathbf{Y_{aux}}$ at the corresponding matrix elements.

Second, the voltage/current distributions can be solved easily with multiple excited voltage ports which is especially true in a converter since noise can propagate from several sources simultaneously. The solving approach is presented in Sec. 4.3.3 by canceling the corresponding columns of the connecting matrix.

Third, it is able to optimize selections and locations of decoupling capacitors and other devices since $\mathbf{Y_{aux}}$ can be treated independently in the model.

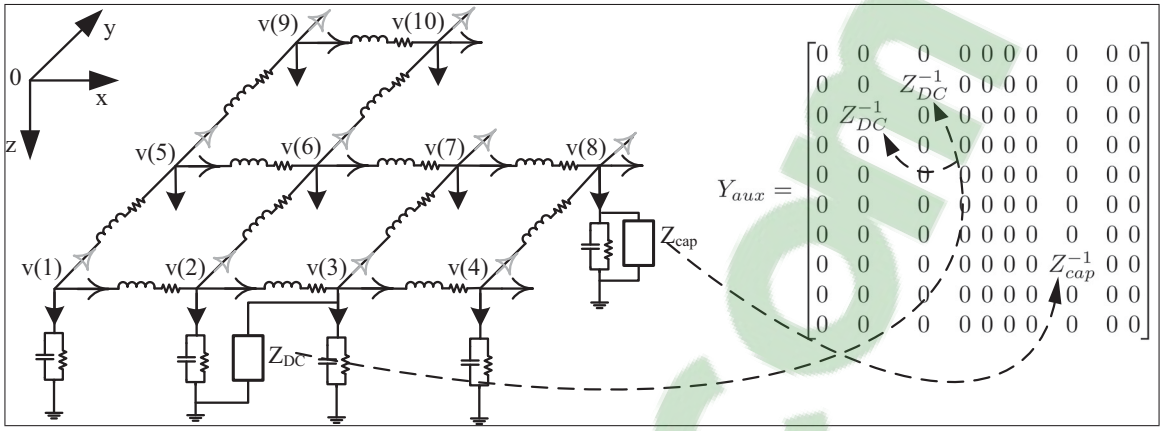


Figure 4.8 2D lumped model with external devices

Fig. 4.8 shows the power rails structure given in Fig. 4.6 with added external devices. In this configuration, a decoupling capacitor is soldered between power and ground plane at cell 8 whereas a DC/DC converter is soldered at cell 2 on ground and cell 4 on power rails. Equivalent impedance of the DC/DC converter and decoupling capacitor are $\mathbf{Z_{DC}}$ and $\mathbf{Z_{cap}}$ respectively. The admittance matrix $\mathbf{Y_{aux}}$ is defined at the right hand side of Fig. 4.8. As shown, the admittance ${\mathbf{Z_{DC}}}^{-1}$ is inserted to $\mathbf{Y_{aux}}$ at $\mathbf{Y_{aux}}(2,3)$ and $\mathbf{Y_{aux}}(3,2)$ whereas ${\mathbf{Z_{cap}}}^{-1}$ is placed at $\mathbf{Y_{aux}}(8,8)$.

4.3.3 Solving approach

In order to compute VTG, the voltage vector, i.e. $\mathbf{V}$, is decoupled to source voltage and distribution voltage vectors, i.e. $\mathbf{V_0}$ and $\mathbf{V_c}$, respectively.

$$\mathbf{V} = \mathbf{V_0} + \mathbf{V_c} \tag{4.24}$$

Assuming that the source voltage is excited at cell e, the source voltage vector is given as:

$$\mathbf{V_0}(p) = \begin{cases} 1 & \text{if} \quad p = e \\ 0 & \text{otherwise.} \end{cases} \tag{4.25}$$

In order to represent (4.13) and (4.14), the new transformation matrices $\mathbf{A_0}$, $\mathbf{A_c}$, $\mathbf{B_0}$, $\mathbf{B_c}$ are created to satisfy (4.26) - (4.27).

$$\mathbf{AV} = \mathbf{A_0 V_0} + \mathbf{A_c V_c} \tag{4.26}$$

$$\mathbf{BV} = \mathbf{B_0 V_0} + \mathbf{B_c V_c} \tag{4.27}$$

$$\mathbf{A_0}(p,q) = \begin{cases} 1 & \text{if} \quad q = p = e \\ -1 & \text{if} \quad q = e = \mathbf{Q_x}(p) \\ 0 & \text{otherwise.} \end{cases} \tag{4.28}$$

$$\mathbf{B_0}(p,q) = \begin{cases} 1 & \text{if} \quad q = p = e \\ -1 & \text{if} \quad q = e = \mathbf{Q_y}(p) \\ 0 & \text{otherwise.} \end{cases} \tag{4.29}$$

$$\mathbf{A_c}(p,q) = \begin{cases} 0 & \text{if} \quad q = e \\ \mathbf{A}(p,q) & \text{otherwise.} \end{cases} \tag{4.30}$$

$$\mathbf{B_c}(p,q) = \begin{cases} 0 & \text{if} \quad q = e \\ \mathbf{B}(p,q) & \text{otherwise.} \end{cases} \tag{4.31}$$

Replacing (4.24), (4.26) and (4.27) into (4.13) - (4.15) yields:

$$\mathbf{I_x} = \mathbf{Y_x}\left(\mathbf{A_0 V_0} + \mathbf{A_c V_c}\right) \tag{4.32}$$

$$\mathbf{I_y} = \mathbf{Y_y}\left(\mathbf{B_0 V_0} + \mathbf{B_c V_c}\right) \tag{4.33}$$

$$\mathbf{E I_x} + \mathbf{D I_y} = \mathbf{Y_z}\left(\mathbf{V_0} + \mathbf{V_c}\right) \tag{4.34}$$

In (4.34), $\mathbf{Y_z}$ is replaced by $\mathbf{Y_{aux}} + \mathbf{Y_z}$ to take the impedance of external devices into the full model, as explained in Sec. 4.3.2:

$$\mathbf{E I_x} + \mathbf{D I_y} = \left(\mathbf{Y_z} + \mathbf{Y_{aux}}\right)\left(\mathbf{V_0} + \mathbf{V_c}\right) \tag{4.35}$$

From (4.32), (4.33) and (4.35), the voltage distribution on the low power rails, i.e. $\mathbf{V_c}$, is computed by:

$$\mathbf{V_c} = (\mathbf{E Y_x A_0} + \mathbf{D Y_y B_0} - \mathbf{Y_z} - \mathbf{Y_{aux}})^{-1}\,\mathbf{T} \tag{4.36}$$

$$\mathbf{T} = (-\mathbf{E Y_x A_c} - \mathbf{D Y_y B_c} + \mathbf{Y_z} + \mathbf{Y_{aux}})\,\mathbf{V_0} \tag{4.37}$$

By injecting a voltage of 1V at the excitation cell, i.e. cell e, the VTG from cell e to a typical cell l is computed as:

$$VTG_{e,l} = \frac{\mathbf{V}(l)}{\mathbf{V}(e)} = \mathbf{V}(l) \tag{4.38}$$

4.4 Experimental results

4.4.1 Experimental setup

In this section, a typical power converter low-power rails structure is analyzed in both computation and experimentation. The circuit and the board layout are depicted in Figs.4.9 (a)–(b), respectively. The part numbers of the devices connected to the plane are summarized in Table. 4.1. As shown in Fig. 0.4, PS1 (typically 12V) supplies PS2, PS3 and PS4 (typically $\pm$15V). These isolated low power converters then supply the power transistor gate drivers. There are 5 footprints on the board's top layer (x1 to x5) for including two types of capacitors, namely film and/or ceramic. The objective is to study the usual capacitor decoupling approach to validate the proposed modeling approach. Both capacitor technologies and their spatial distribution effects on VTG are studied to provide a comprehensive validation. There is also one footprint on the board (x6) to include a ferrite bead (B1), a device typically used to solve noise problems at board level. As mentioned in Section. , VTGs between each devices (PS1 and PS2, PS1 and PS3...) are essential for quantifying the noise propagation in the low power rails. VTGs are extracted experimentally based on scattering parameters, a standard function on every VNA. Scattering parameters are then converted to VTG by the procedure described

in Appendix I. For the remainder of this section, the focus will be set on the VTG between PS2 and PS1, the other VTGs being obtained in the same way.

4.4.2 2D lumped model parameters identification

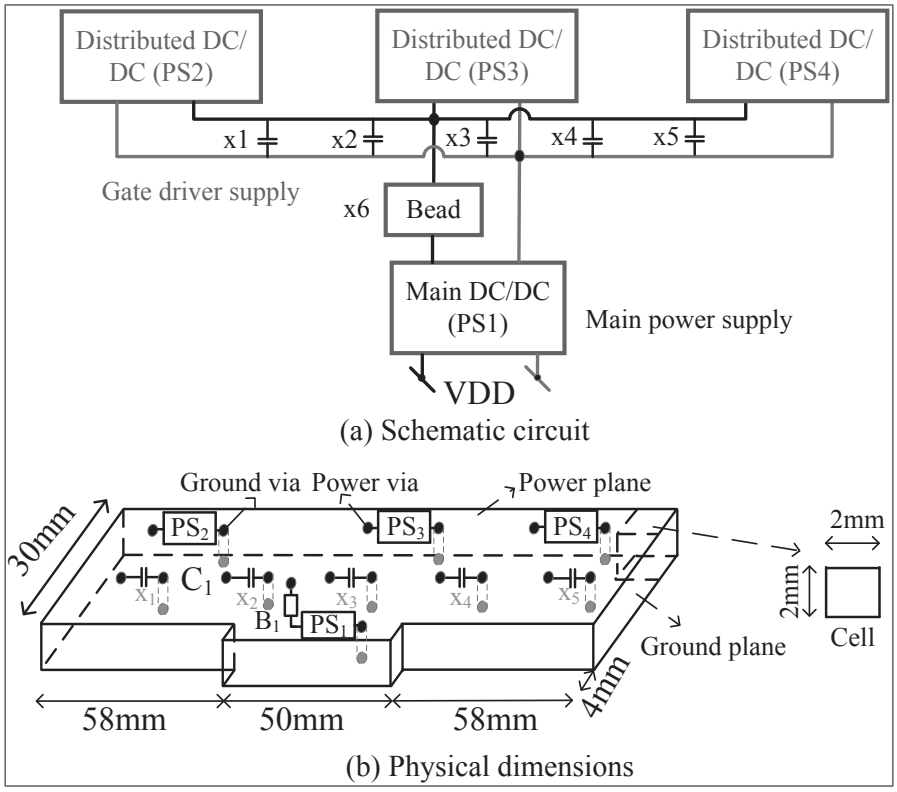


Figure 4.9 Prototype of low power rails

Prior to computing VTG, parameters are needed for both the low power rails and external components. First, the low power rails is divided into small cells whose dimensions must be less than 15cm corresponding to the highest considered frequency of 100MHz following the condition discussed in Sec. 4.3. Based on numerical investigation, using square cells of 2mm $\times$ 2mm ensures good precision up to 100MHz, yielding to the following cell parameters:$R_x = R_y = 0.96m\Omega$, $L_x = L_y = 1.8831nH$ and $C = 0.1134pF$ according to (4.1).

Second, external devices impedance must be measured to complete the model. This task is performed using an Agilent Network Analyzer E5061B. Impedance of PS1, PS2, C1 and B1 are

Table 4.1 List of external devices

Designator	Manufacturer	Part Number
PS1	TRACOPOWER	THN 15-4812WI
PS2, PS3, PS4	CUI Inc	VASD1-S12-D12-SIP
C1	EPCOS (TDK)	B32529C104J
B1	TDK	HF30ACC453215-T

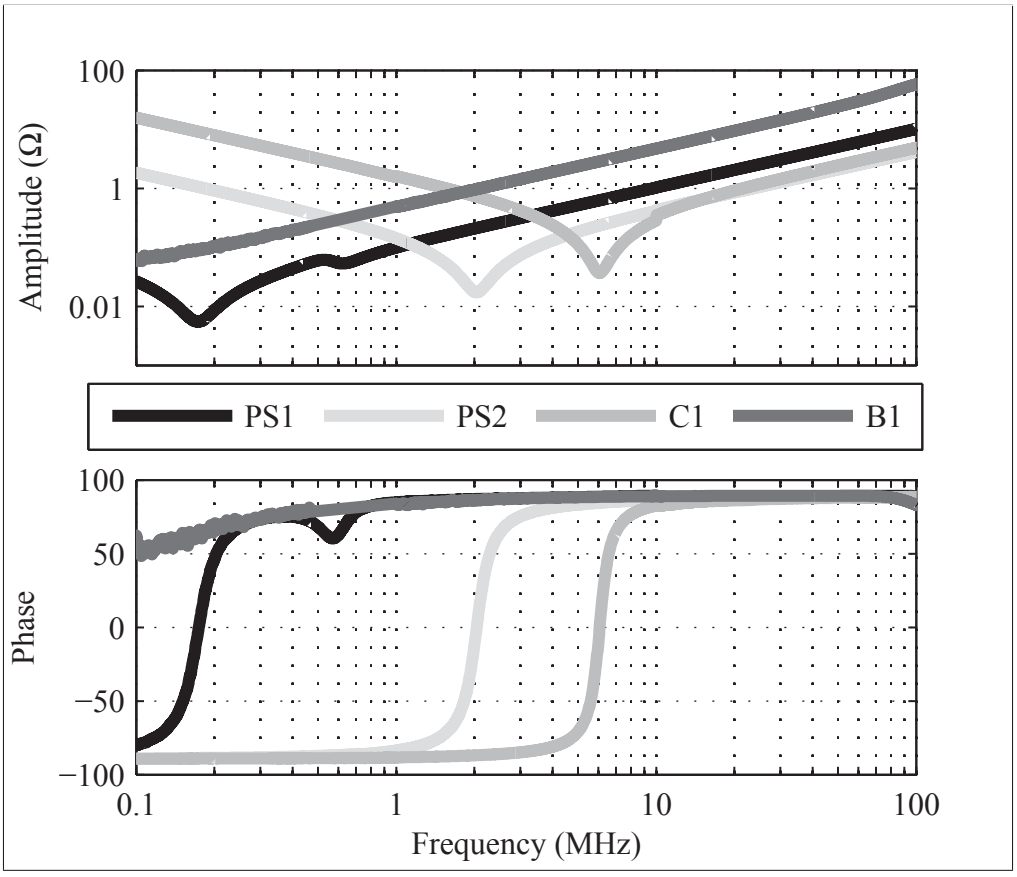


Figure 4.10 Measured impedance of external devices

presented in Fig. 4.10. As shown in Fig. 4.10, impedance of PS1, PS2 and C1 are capacitive at low frequency and inductive at high frequency. The resonant frequencies are 200kHz, 2.2MHz and 6MHz, respectively. The impedance of PS1 is the lowest at frequencies below 1MHz and the highest at frequencies above 10MHz. The effects of all external devices on VTG is presented in the next sections.

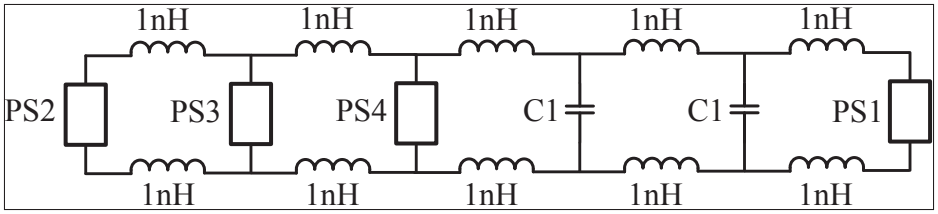
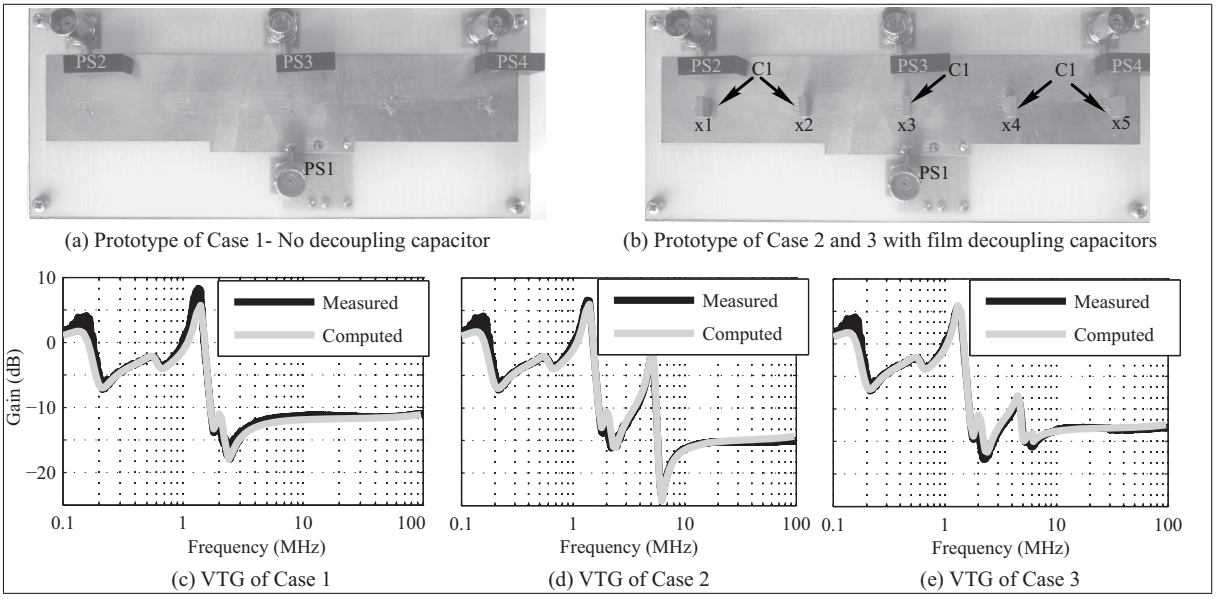


Figure 4.11 1D lumped model neglecting low power rails



(a) Prototype of Case 1- No decoupling capacitor

(b) Prototype of Case 2 and 3 with film decoupling capacitors

(c) VTG of Case 1

(d) VTG of Case 2

(e) VTG of Case 3

Figure 4.12 VTG of low power rails for different cases of decoupling capacitors

4.4.3 VTG with decoupling capacitors

In order to validate the proposed modeling approach, the spatial distribution of decoupling capacitors on VTG is analyzed. In order to do this comparison, two decoupling capacitors are inserted in different rooms of the low power rails and the VTG is computed from 100kHz to 100MHz. For comparison basis, a lumped model neglecting the low power rails is used. This model, shown in Fig. 4.11, includes the impedance of PS1, PS2, PS3, PS4 and two decoupling capacitors C1. To account for the leads of the components, a small connecting inductance of 1nH is added. VTG for the both models is shown in Fig. 4.13. Three cases are presented for the low power rails:

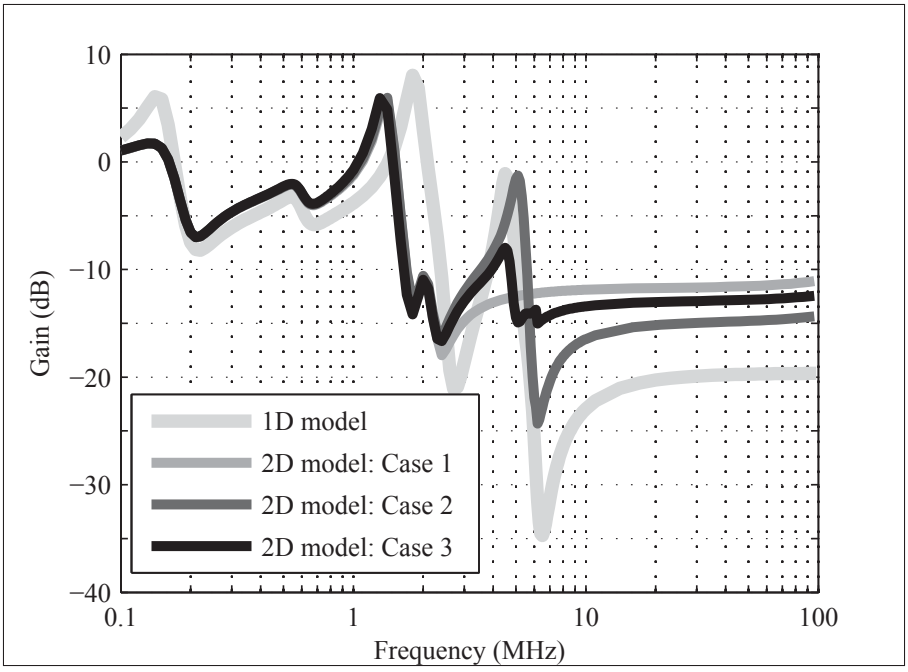


Figure 4.13 Computed VTGs from PS1 to PS2

Case 1 - no decoupling capacitor is used.

Case 2 - decoupling capacitors are inserted at x1 and x2.

Case 3 - decoupling capacitors are inserted at x4 and x5.

As depicted in Fig. 4.13, VTGs are the same for each of the three cases below 2.5MHz. This means that VTG in this frequency range is managed by the impedance of the devices in the circuit, while the influence of the low power rails is negligible. Over 5MHz, a clear influence of the low power rails is observed. First, the VTG is quite different from the 1D lumped model. Clearly, the low power rails has a lower impedance compared to the 1D lumped model, which imposes an higher transfer gain. This is a major factor for considering a 2D model rather than a 1D model. Also, this experiment clearly shows how the position of the decoupling capacitors impacts on the VTG. Intuitively, including capacitors in rooms x1 and x2 should decrease the VTG since these decoupling capacitors are directly in the current path between PS1 and PS2. At high frequency, these capacitors bypass an important part of the current reducing the collected voltage on PS1 and thus the VTG. This behavior can be observed over

10MHz, where VTG is lower for capacitors in rooms x1 and x2, compared with rooms x4 and x5. The influence of the low power rails is remarkable between 2.5MHz and 10MHz. Without decoupling capacitors, a purely resistive behavior of the low power rails is observed. However, with decoupling capacitors, two resonances which have a strong impact on VTG, are observed. For exactly the same capacitor parameters, these resonances appear at different frequencies with different amplitudes, which emphasize the influence of the low power rails. Of course, this behavior cannot be predicted by using a 1D model. The experimental validation is shown in Fig. 4.12 with the prototype. As observed in the figure, experimental results closely match with computations for all cases.

4.4.4 VTG with ferrite beads

With the best experience of authors, ferrite bead and LC filter provide high attenuation on VTG that can exceed the precision of measurement devices, hence, provide difficulty to verify computation by measurement. Since the purposes of this section are to validate computational model and study the effect of EMI attenuators, a ferrite bead, i.e. B1, which provides a reasonable attenuation level is chosen to analyzed without losing generality. The experimental results are shown in Figs. 4.14 and 4.15 with different combinations of decoupling capacitors and ferrite beads as following cases:

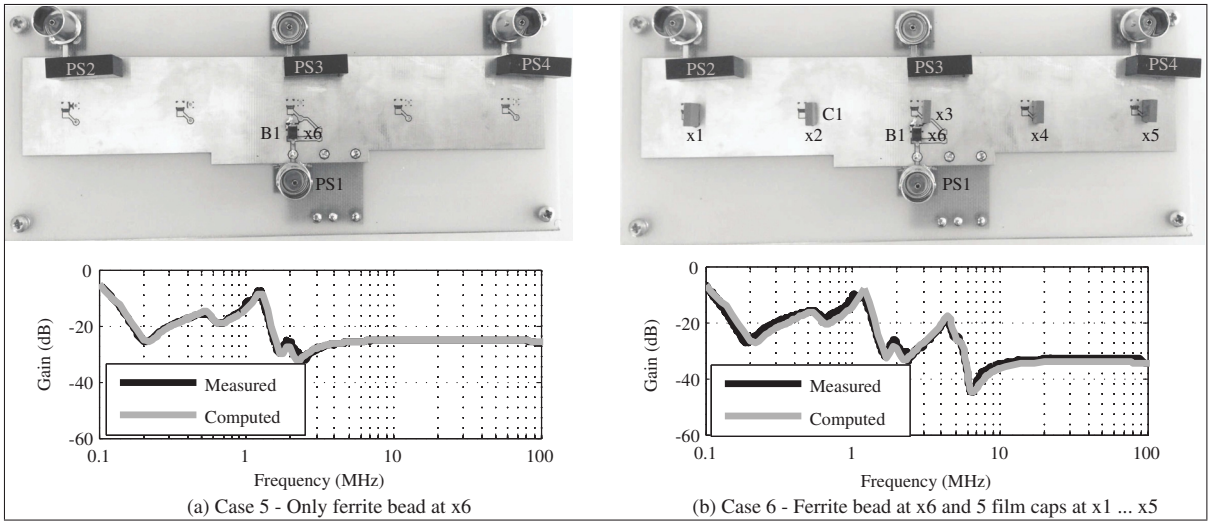
Case 1 - Without decoupling capacitors.

Case 4 - 5 decoupling capacitors at x1, x2, x3, x4 and x5.

Case 5 - Only ferrite bead at x6.

Case 6 - Ferrite bead at x6, 5 decoupling capacitors at x1, x2, x3, x4 and x5.

Fig. 4.14 shows the experimental prototypes and corresponding VTG of low power rails with EMI attenuators such ferrite bead and combination of ferrite bead with 5 film capacitors. There are good agreements between computation and measurement proving the accuracy of proposed computational model. The influence of ferrite bead on VTG of low power rails is analyzed



(a) Case 5 - Only ferrite bead at x6

(b) Case 6 - Ferrite bead at x6 and 5 film caps at x1 ... x5

Figure 4.14 VTG of low power rails with different combinations of ferrite bead

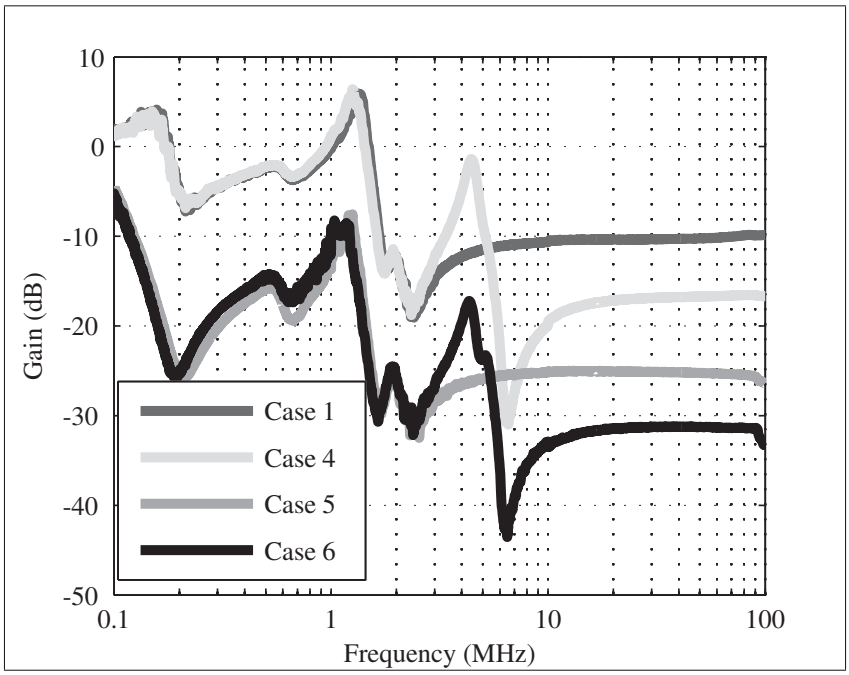


Figure 4.15 Experimental results with bead and film capacitor

through the comparison between different EMI attenuating configurations given in Fig. 4.15. As can be observed, the ferrite bead is effective to attenuate VTG of 20dB in all considered frequency ranges. It is resulted by the relationship between impedance of B1 and PS1 while they are connecting serially. First, impedance of B1 is 10 times higher than that of PS1. Also,

B1 impedance's phase is positive as that of PS1. It is experienced that higher impedance ferrite bead is, higher attenuation achieved. However, the power density is reduced meanwhile. On the other hand, the noise attenuating ability of ferrite bead decreases below 200kHz since it has opposite impedance phase as PS1.

The combination of ferrite bead and film decoupling capacitors provides $6dB$ higher attenuation than only ferrite bead in frequency of 5MHz – 100MHz. However, this combination also results VTG gain in frequency range of 2.2MHz – 5MHz due to negative phase impedance of film capacitor. Those effects of decoupling film capacitors are analyzed in previous section. The fast computing time which is an advantage of the proposed approach is shown in Table 4.2.

Table 4.2 Computing time of the proposed method

CPU	Intel(R) Core(TH) i7 @3.4GHz
RAM	8GB
Number of cell	1312
Number of sampling frequency	211
Computation time (sec)	121

4.5 Conclusion

In this chapter, a modeling strategy for computing VTG between port pairs of low power rails of power converters with external devices is proposed. Placing real impedance of external devices into the model as an additional matrix adds flexiblity for modifying external devices, in terms of type, number and location. The precision of the proposed model is proven by the experimental results, which also show the effects of decoupling capacitors to VTG. According to the impedance of the decoupling capacitors and other devices, both VTG attenuation and amplification can be observed. The proposed model is well suited to avoid the impedance mismatch resulting in VTG amplification. Moreover, the proposed approach is flexible and precise for optimal design of the low power rails. This point will be considered in future work.

CHAPTER 5

APPLICATION OF Y-CAP ON NOISE ATTENUATION IN LOW POWER PARTS OF POWER CONVERTER

Chapter summary

As presented in the previous chapters, noise propagation in the low power rails is difficult to managed (Chapter 4). Even though the filter can be designed based on the advanced model such GIR (Chapter 3) to prevent noise passing to the functional circuit, it will be more effective to further attenuate noise before it arrives at the low power rails. In this chapter, a novel Y-capacitor, herein shorted as Y-cap, utilization approach is proposed to attenuate the high frequency - voltage oscillation on the Gate driver power supply, V_{DCin}. The Y-cap is used to connect the input of Gate driver DC/DC converter and the negative rail of the DC bus, providing a low impedance path for high frequency noise to complete its loop in the high power circuit while reducing its portion propagating to the low power circuit. As a result, the high frequency spikes on components in the low power circuit will be attenuated. The proposed approach is effective to improve noise performance of a converter at the final stage design and maintenance phase. Furthermore, to make the approach useful in general practical conditions, an intuitive design method based on voltage measurement only is introduced. It helps to avoid difficult and costly impedance measurement in high frequency. To support the analysis, experiments of a prototype buck converter with a typical H-bridge driver circuit are performed. Several combinations of Y-caps are used to prove the effectiveness of the proposed method. The contents of this chapter was published in *IEEE Proceeding of ICIT 2017*, March 2017 (Nguyen & Blanchette, 2017).

5.1 Introduction

The noise current i_G in the gate driver, shown in Fig. 5.1, is generated during the switching transients of the power transistors (from ON to OFF and OFF to ON states) (Clemente *et al.*, 1987; Jin & Weiming, 2006). It results in high frequency voltage oscillations on the DC/DC

gate driver of a H-bridge creating critical impact on component reliability and control quality. This high frequency oscillation can propagate to the other parts of low power circuit following the dashed line, as shown in Fig. 5.1, creating voltage spikes on components (Nguyen *et al.*, 2017c). Depending on parasitic parameters of power transistors and PCB layout, the voltage spike frequency can be in the range of 10MHz - 100MHz. Taken into account the 5% rejection margin DSP and very poor PSRR of op-amp and comparator, as discussed in Section. 2.1, voltage oscillation on Gate driver power supply can alter the functionalities of other devices in the low power circuit. Therefore, attenuating noise on the Gate driver power supply and its propagation on the low power rail is mandatory to ensure power converter reliability.

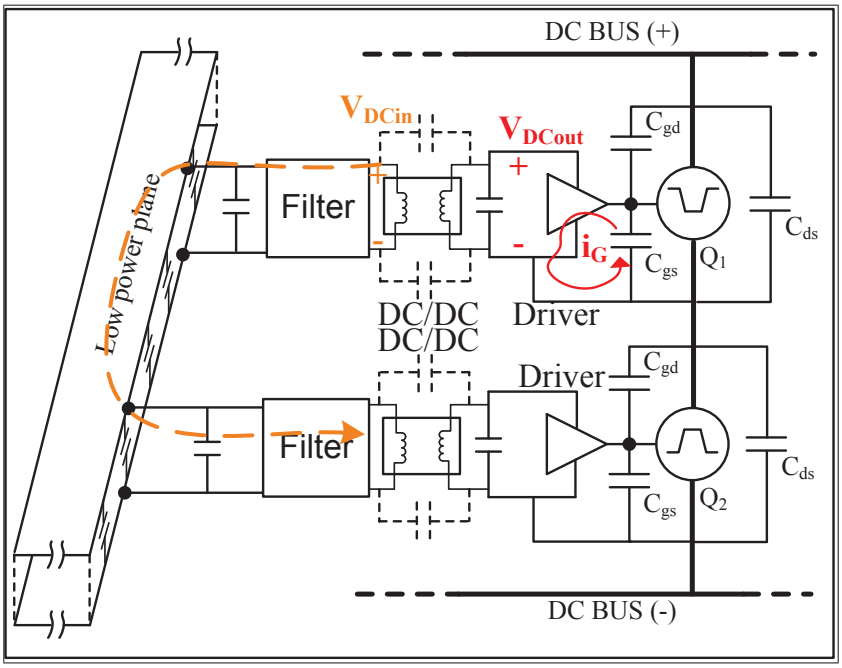
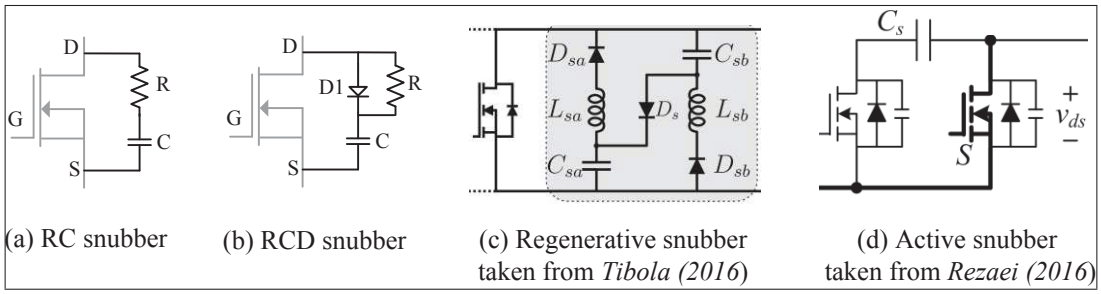


Figure 5.1 Noise propagation path

Unfortunately, the LC filter performance degrades significantly in frequency range above 30MHz due to the limit of components. On the other hand, EMI attenuator placements on the low power plane to obtain high attenuation of noise in high frequency is a difficult challenge for designers. Therefore, it is more convenient to attenuate noise at the DC/DC gate drive power supply, specifically V_{DCin}, before it propagates into the power rail.

Several snubber configurations have been developed to reduce the voltage ringing on Drain - Source V_{DS} of the power transistor (Popović-Gerber & Ferreira, 2012; Chen *et al.*, 2016; Tibola *et al.*, 2016; Dong *et al.*, 2016; Rezaei *et al.*, 2016), are summarized in Fig. 5.2.



(a) RC snubber (b) RCD snubber (c) Regenerative snubber taken from *Tibola (2016)* (d) Active snubber taken from *Rezaei (2016)*

Figure 5.2 Snubber configurations

The usual configuration is RC snubber (Popović-Gerber & Ferreira, 2012) with power dissipation on the damping resistor. The RCD snubber is often used to limit power dissipation (Chen *et al.*, 2016) and regenerative snubber to further improve the efficiency (Tibola *et al.*, 2016). However, due to the fact that the damping resistor always exists and it absorbs high inrush current at the rising and falling edges of the power transistors, the power consumption can not be completely eliminated. With the recent development of SiC devices (Popović-Gerber & Ferreira, 2012; Rondon-Pinilla *et al.*, 2014), the power consumption by snubbers is increased significantly with high switching frequency, and the ratio of switching and snubber conduction frequencies. Then, efficiencies of mid- and low-power power converters are reduced. In addition, for high power application, the RC - type snubber must be designed with high power rating which requires space and increases cost. The recent development of active snubber (Rezaei *et al.*, 2016) are useful to further reduce the power loss. However, additional switching devices, including their gate driver and control circuits complicate the converter circuit and degrade reliability. Moreover, it is not encouraged in commercial applications due to additional cost.

These facts show that snubber is not the best solution to eliminate voltage spike across power transistors. Consequently, the high frequency voltage oscillations still appear in the low power

circuit, as previously discussed. It is motivated to develop an approach to attenuate noise at the input of Gate driver DC/DC converter using Y-cap. This approach is presented in this chapter.

So far, the Y-cap have been used between line - to - ground to suppress the common mode voltage (Shin & Lee, 2012) by providing a low - impedance path to the ground or chassis (Gustavsen & Nicollet, 2001; Zhou *et al.*, 2016). This Y-cap can result in a dangerous leakage current which is not acceptable for applications such as medical instruments and human interface (Bai *et al.*, 2017). At board level, it is suggested to reduce common mode noise from output to input of the DC/DC converter (Power, 2015) to meet EMI standards.

In this chapter, the Y-cap is employed to attenuate high frequency noise current propagating to the low power circuit, resulting in voltage spike on the components such as input of gate driver DC/DC converter. More specifically, the Y-cap is used to provide a low - impedance path for high frequency current to propagate to the high power circuit, reduce its impact on the low power circuit. Furthermore, to make the approach useful in general practical conditions, an intuitive design method based on voltage measurement only is also introduced. It helps to avoid difficult and costly impedance measurement in high frequency. The proposed method has several advantages.

Why Y-cap?

In this application, the Y-cap is used instead of X-cap to guarantee the voltage isolation between high and low power circuits, which is a mandatory safety requirement for power converter design. In failure condition, Y-cap fails open, giving no impact on the normal converter operation. Instead, the X-cap usually fails short. This short circuit is an ideal path for high current in high power circuit to flow to the low power circuit, where the current and voltage ratings of components are low. Consequently, the low power circuit and the complete converter will be damaged. Moreover, the user can also experiment an electric shock.

In addition, the Y-cap has several advantages to be used in the proposed approach. First, the Y-cap is efficient to absorb high frequency current due to its low ESL. Second, power dissipation

on Y-cap is negligible due to its very small ESR, so there is no impact on the power converter efficiency. Third, Y-cap can be added to the existed circuit without changing the layout of converter circuit. Therefore, the proposed method is effective to employ at the last stage of converter design process or to improve noise profile of the converter in maintenance phase.

Is Y-cap selection trivial?

Even though Y-cap has been widely used in practical designs, selection of Y-cap for noise attenuation in low power circuit is not trivial.

As pointed out in Sec. 2.2.3, where the smaller impedance with positive phase results in higher noise, the phase of impedance has a strong impact on noise performance. The role of the impedance phase is also confirmed by the VTG performance presented in Sec. 4.4.4, where the opposite phases of ferrite bead and DC/DC converter create higher VTG than the case of no ferrite bead. Moreover, the experiment in Sec. 2.3.2 shows the fact that total impedance seen from the gate driver, i.e. parasitic capacitance of DC/DC converter and cables, has more direct effect on noise performance than the parasitic capacitance alone. Therefore, the Y-cap must be chosen for minimizing the total impedance of the noise propagation path. This selection will be presented in details by the proposed method.

This chapter is organized as follows. Sec. 5.2 analyzes the gate current created in transient states and voltage oscillation at Gate driver power supply. Sec. 5.3 presents the proposed Y-cap configuration for noise attenuation purpose. Sec. 5.4 provides the experimental results of several Y-cap combinations followed by the conclusion in Section. 5.5.

5.2 Voltage oscillation on gate driver DC/DC converter analysis

In this section, the origin of high frequency voltage oscillations on DC/DC gate driver is analyzed based on switching sequences (Clemente *et al.*, 1987). Fig. 5.3 shows the high frequency model of a Gate driver circuit of a MOSFET in a typical Buck converter. It consists of mod-

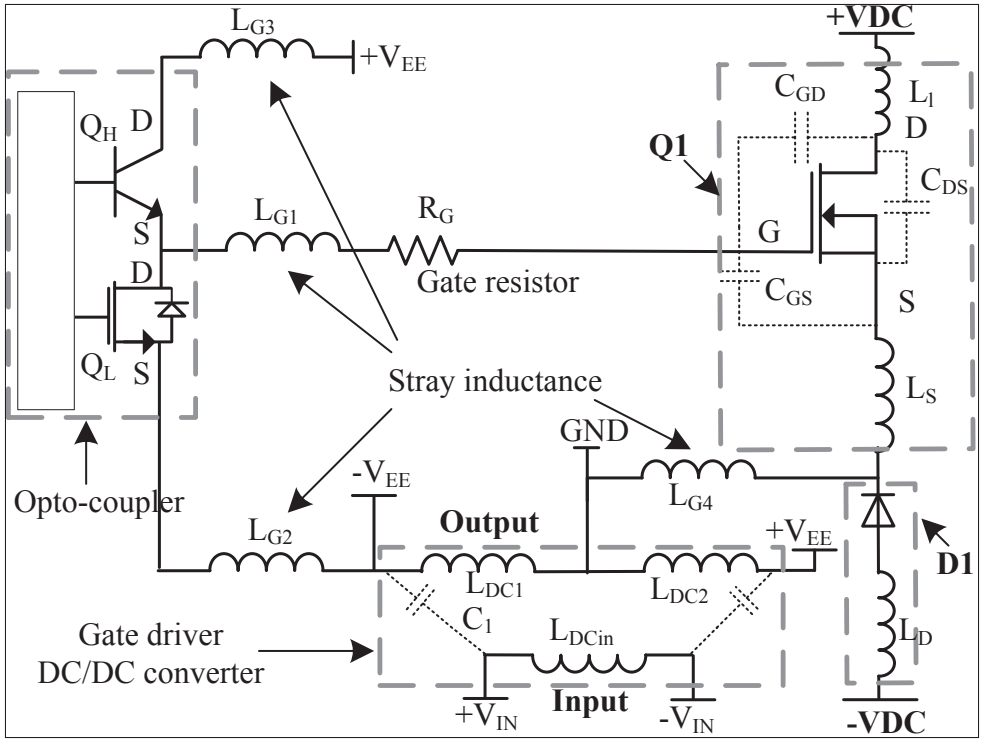


Figure 5.3 High frequency model of the triggering circuit

els of the output of Opto-coupler, MOSFET, Diode and Gate drive DC/DC converter. In this figure:

- The high - side MOSFET Q_1 is modeled with Miller capacitor from Drain to Gate, C_{GD} and input capacitor C_{GS}. The internal gate resistance and the external gate resistor are summed as R_G. L_l is the stray inductance of PCB traces connecting the Drain to +VDC and internal drain leakage inductance. L_S presents the internal leakage inductance;

- The diode D_1 is presented by L_D, which is the sum of internal leakage inductance and stray inductance of the trace connecting D_1 to the negative DC bus rail;

- From measurement observations, DC/DC converter, U_1, is considered as a 5 pins network with inductive impedance between pins at the same sides, i.e. L_{DCin} as inputs and L_{DC1}, L_{DC2} as outputs; and parasitic capacitance, C_1, C_2, ..., from inputs to outputs;

- L_{G1}, L_{G4}, L_{G2} and L_{G3} represent the PCB traces stray inductances connecting the opto-coupler leads to Q_1 and U_1.

During the switching operation, the high frequency current is created at the turn - off delay interval 3 of Q_1 (Clemente *et al.*, 1987). In this interval, the current in the driver circuit is superimposed to the current passing through C_{GD} and discharging current of C_{GS}:

$$i_G(t) = i_{GD}(t) + i_{GS}(t) \tag{5.1}$$

It is worth noticed that the common mode noise is not considered in this model to keep the analysis simple. There are varieties of common chokes with high impedance at high frequency (up to 100MHz) for common mode filter purpose. In contrast, it is more challenging to design differential filters due to degraded performances of components at high frequency. In fact, ferrite beads are often used for this application, but their interaction with capacitive device such as DC/DC converter must be carefully taken into account due to the analysis presented in Sec. 4.4.4.

5.2.1 Current through Miller capacitor, i_{GD}

A change of drain current creates voltage variation on L_l, which further produces the current i_{GD} flowing to the Gate through C_{GD}. The current path is shown in Fig. 5.4. The current passes through the gate resistor R_G, stray inductance L_{G1} between the opto-coupler and the transistor gate, low transistor Q_L of the opto-driver push - pull output, stray inductances L_{G2} and L_{G4}, negative outputs of DC/DC converter L_{DC1} before completing the loop by passing the MOS-FET DS junction through its source leakage inductance L_S. This current produces the voltage ringing between pins -VEE and GND of the output DC/DC converter, i.e. V_{rd}. Following good PCB practices, all stray inductances are designed as low as possible. Considering the fact that C_{GD} is a small capacitance, e.x. few hundreds pF, the frequency of voltage ringing, specified as f_d hereafter, is very high. The amplitude of V_{rd} depends on the drain current variation, di_D/dt, instantaneous drain current i_D, duty cycle, L_l and C_{GD}. With very high speed switching

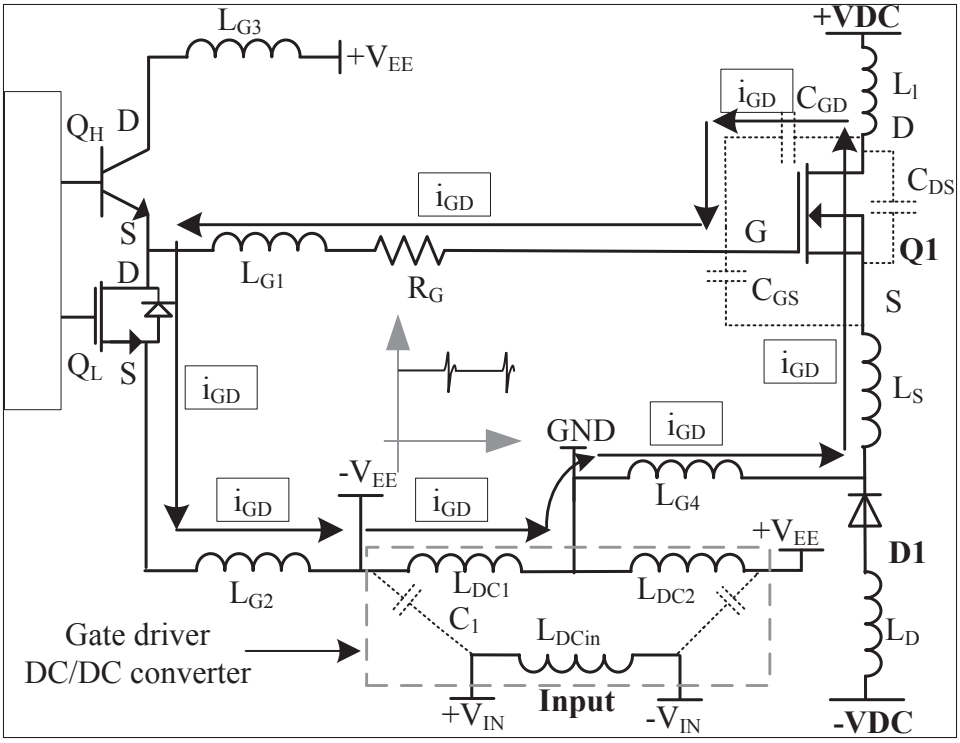


Figure 5.4 Current path of i_{GD}

devices such GaN and SicMOS , di_D/dt is increased significantly, further increasing amplitude of voltage oscillations on the DC/DC converter.

5.2.2 Discharging current of Gate - Source Capacitor, i_{GS}

During turn-off delay interval 3 of Q_1, the Gate capacitor C_{GS} starts to discharge through the Gate resistor. The current path is shown in Fig. 5.5. Current passes through all the Gate impedances, Q_L of opto-coupler, the negative rails of DC/DC converter (-VEE) and finishes the loop at the Source of Q_1. Once the PCB layout is completed, the amplitude of i_{GS} depends only on the gate capacitance ($i_{GS} = C_{GS}\frac{dV_{GS}}{dt}$) and the gate voltage. However, it is independent of the converter operating points, i.e. duty cycle or DC bus current.

Considering the fact that C_{GS} is higher than C_{GD} for MOS devices, the oscillation frequency created by i_{GS}, specified as f_s hereafter, is lower than f_d.

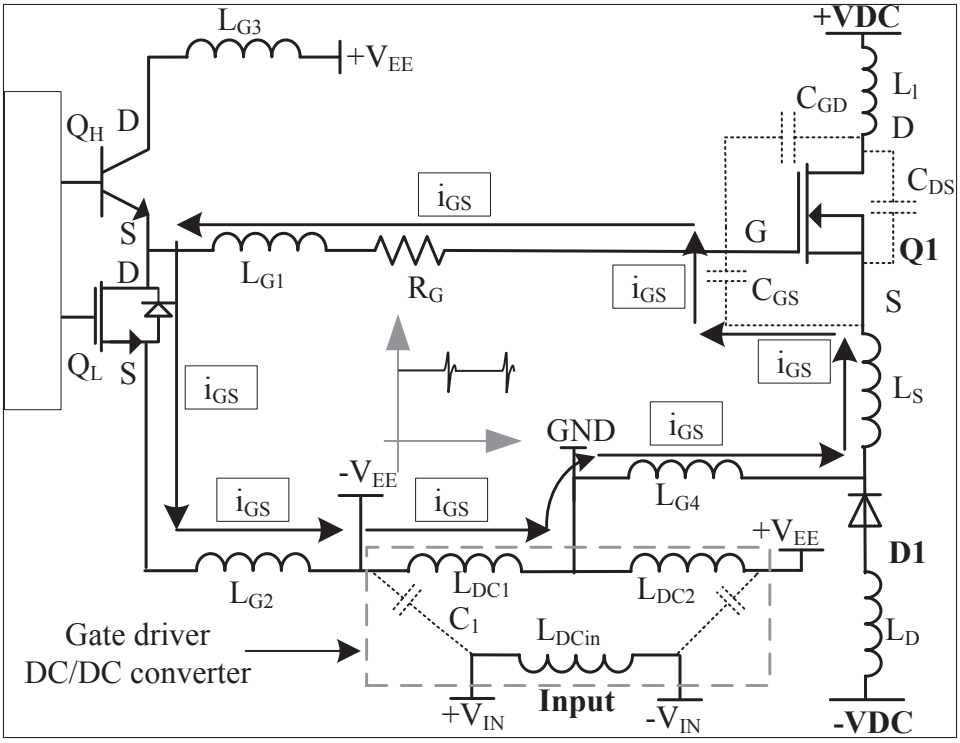


Figure 5.5 Current path of i_{GS}

5.2.3 Voltage oscillation on DC/DC converter inputs

The analysis of i_{GD} and i_{GS} in Sec. 5.2.1 and 5.2.2 are done without considering the isolated capacitance of the DC/DC converter to simplify the circuit. Taken into account this parasitic element, the current $i_G = i_{GD} + i_{GS}$ in the gate driver circuit has 2 paths to propagate, as shown in Fig. 5.6. The first part, namely i_{G1} passes through L_{DC1} and L_S to complete its return path at the Source of Q_1, whereas the second part i_{G2} passes through the DC/DC converter parasitic capacitance to its inputs. On the low power rail, i_{G2} propagates within complex paths to the other functional circuits. It results in high frequency voltage oscillation on components (Nguyen *et al.*, 2017c), including V_{DCin} on the Gate driver DC/DC inputs.

As a result, V_{DCin} contains the oscillations at 2 different frequencies namely i_{GD} and i_{GS}, presented as $V_{DCin} = V_{DCd} + V_{DCs}$. The worst case of high frequency voltage oscillation considered in this case is V_{DCd} at frequency of f_d. Note that this justification comes from experimental

observation. Detailed quantification of noise propagating between the output and input sides based on complete model of DC/DC converter is out of scope of this chapter.

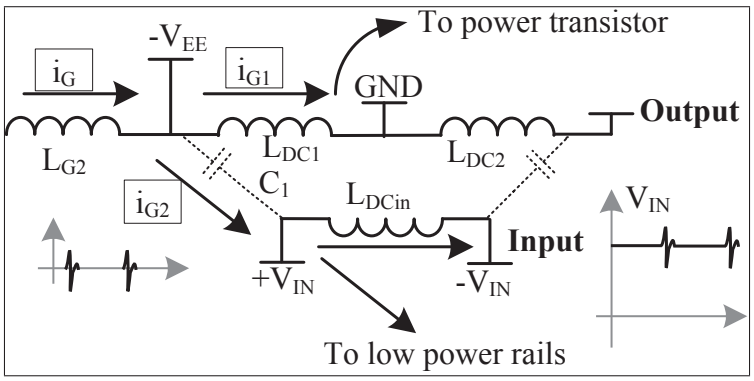


Figure 5.6 Current sharing at Gate driver DC/DC converter

5.3 Proposed Y-cap application on noise attenuation in power converter

As pointed in Sec. 5.2, the noisy current i_{G2} can create voltage oscillations on components in the low power rail and other functional circuits, specifically V_{DCin} at the inputs of the DC/DC converter. While the low frequency part, V_{DCs}, can be attenuated by usual EMI filters (such as decoupling capacitors), the high frequency part, V_{DCd}, is difficult to manage due to the limit of EMI filter components.

In this section, we propose to use Y-cap to attenuate the amplitude of V_{DCd} by providing a return path for i_{G2} to the Source of Q_1. The proposed Y-cap structure is described in Fig. 5.7. In this circuit, C_{Y1} is connected between the input and output of the gate driver DC/DC whereas C_{Y2} is connected between input of gthe ate driver DC/DC to the negative DC bus terminal, -VDC. C_{Y1}, C_{Y2} and L_D form a low impedance current return path for i_{G2}, namely i_{CY} to propagate to the high power circuit. Another part of i_{G2}, namely i_{lpl} travels to the low power rail. This current has complex paths to propagate inside the low power circuit, including L_{DCin} of the gate driver DC/DC, resulting in voltage spikes on components. However, the Y-cap path is designed to have smaller impedance than that of the low power rail, consequently i_{lpl} is reduced. As a

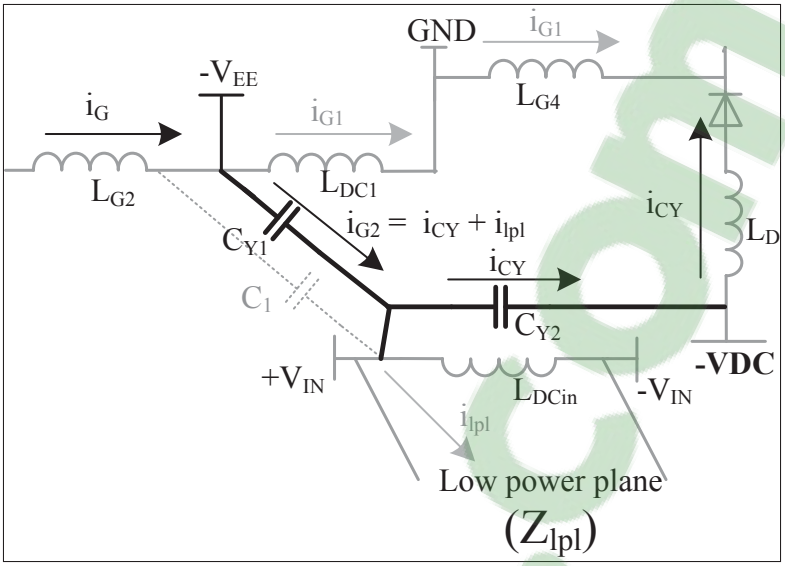


Figure 5.7 Proposed Y-cap circuit to attenuate high frequency noise

result, voltage spike on L_{DCin}, i.e. V_{DCd}, and the remaining parts of the low power rail will be attenuated. Design of these two Y-caps must be done carefully for the following reasons:

1. C_{Y1} is connected between -VEE and +VIN of the DC/DC converter. One observes that C_{Y1} is in parallel with the parasitic capacitor between the input and output of U_1, i.e. C_1. Depending on its capacitive value , which is specific for each DC/DC converter, C_1 can play the similar role as C_{Y1}. Capacitance of C_{Y1} must be limited to avoid the impact on the main switching circuit. In addition, C_{Y1} is also limited to avoid the inrush charging current which could create a high peak on V_{DCd}. In the case that high capacitance C_{Y1} is required, it is a good practice to limit the charging current of C_{Y1} by a small resistor to achieve the best performance;

2. C_{Y2} is used with C_{Y1} to minimize the total impedance of the branch including C_{Y1}, C_{Y2} and L_D as described by (5.2).

$$Minimize\ Z_{CY} = |Z(C_{Y1}//C_1) + Z(C_{Y2}) + Z(L_D)| \tag{5.2}$$

As shown in Fig. 5.7, there are paths inside the gate driver ($L_{DC1} + L_{G4}$) and the low power plane seen from the input of the DC/DC converter (Z_{lpp}). In order to effectively concentrate the high frequency current on the branch of Y-caps ($i_{CY} \gg i_{lpl}$), this branch impedance must have a positive phase, and smaller amplitude than that of the low power rail, ($Z_{CY} \ll Z_{lpl}$), and the path inside gate driver circuit, ($Z_{CY} < Z[L_{DC1} + L_{G4}]$). In general, these impedances are inductive in high frequency range. For instance, the output capacitor of the DC/DC converter becomes inductive in frequency range over 10MHz due to its ESL. In addition, following good practice design, a common mode filter can be used on the low power plane at the input of the DC/DC converter, providing highly inductive impedance seen from that point. Thus, impedance phase of the branch including Y-caps should be positive to have good current sharing with those branches. Instead, a negative phase impedance may increase current in other branches due to the complicated current sharing between opposite phase impedance. C_{Y1} and C_{Y2} can be a single Y-cap or a combinations of several Y-caps selected to minimize the total branch impedance as generally described by (5.2). It is worth noticed that the leakage inductance of Y-cap must be taken into account;

3. Instead of +VIN, Y-caps can be connected to -VIN with the same effects.

Considering the difficulty of extracting small leakage inductance and capacitance values at high frequency and variations in the manufacturing process, we also propose an intuitive approach to design C_{Y1} and C_{Y2}, as presented in Fig. 5.8. In this approach, only voltage measurement is required instead of complex and costly impedance measurement.

5.4 Experimental Results

In this section, a buck converter shown in Fig. 5.9 is used to analyze the effect of Y-cap on noise attenuation. The DC bus is powered by a commercial DC power supply by 50V (at +VDC and -VDC). The main gate driver DC/DC converter (DC1) converts the DC bus to +12V rail supplying the gate driver DC/DC converter. The experiment is performed in open

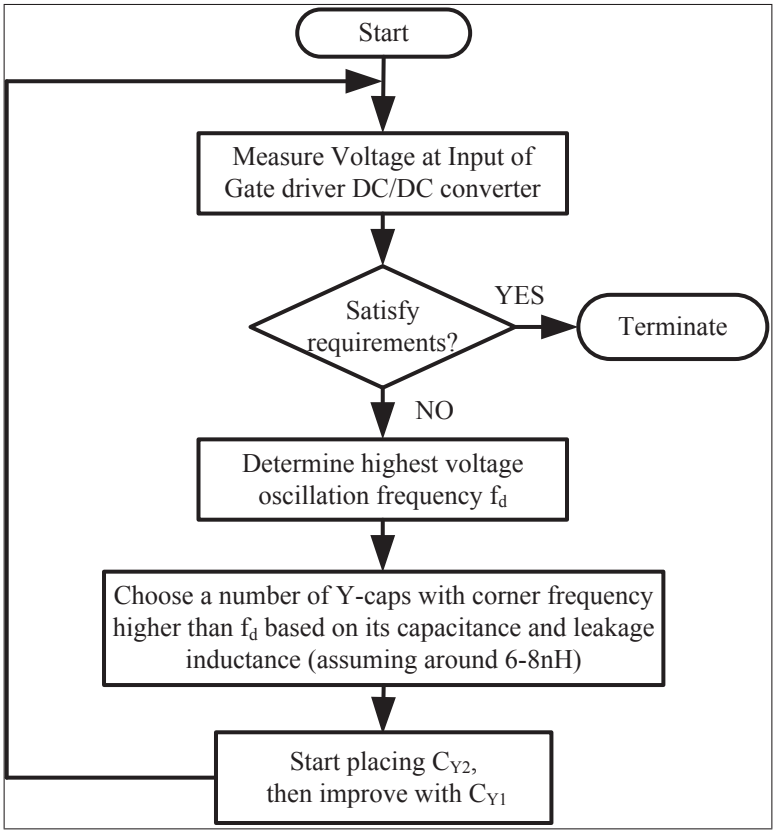


Figure 5.8 Proposed method

loop with fixed duty cycle, so that the sensor and controller circuit are not included to simplify the analysis. The gate drive DC/DC converter is employed to convert the +12V source to $\pm 12V$ supplying the Opto-coupler (HCPL3120) which drives the MOSFET (IRFP450) gate. The control signal for Opto-coupler is provided by an open loop signal generator. The operation parameters of the converter are summarized in Table. 5.1. The experimental setup is placed on a wooden table without metallic parts to keep the common mode noise as low as possible.

Table 5.1 Operational parameters of Buck converter

Input Voltage (V)	**Load** (Ω)	**Switching frequency** (kHz)	**Duty Cycle** (%)
50	5	100	65

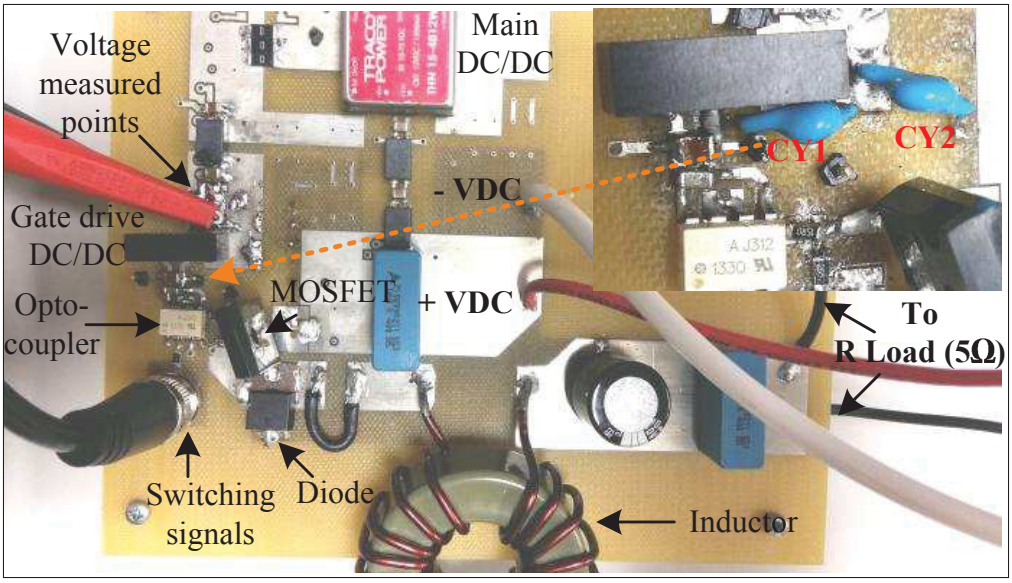


Figure 5.9 Experimental prototype of Buck converter

The purpose of these experiments is to validate the voltage oscillation at the input of the gate driver DC/DC, V_{DCin}, with different configurations of Y-cap. Since the voltage probe touches the circuit, its impedance may contribute significant errors at high frequency. In fact, a voltage probe is terminated by a standard 50Ω resistor inside the oscilloscope. However, impedance of the probe including cable's inductance and probe's internal capacitance, is usually high compared to the gate driver's components. It can significantly impact on the voltage measured. In order to minimize the errors in measurement, a differential probe with small capacitance, approximately $40pF$, has been used. The cable is twisted and probe's legs are placed together without surface area to minimize the mutual inductance. In addition, only one channel of the scope is used for measurement to avoid the common mode current propagating between the oscilloscope channels.

Fig. 5.10 summarizes the experimental results of the input DC/DC voltage, V_{DCin}, with differential combinations of Y-caps. Firstly, the waveform of V_{DCin} without Y-cap is shown in Fig. 5.10a. One observes that the oscillation is superimposed by 2 major parts at frequencies of $f_s = 17$MHz and $f_d = 60$MHz, which follow the analysis presented in Sec. 5.2. The most dangerous peak is the 550mV oscillation at 60MHz.

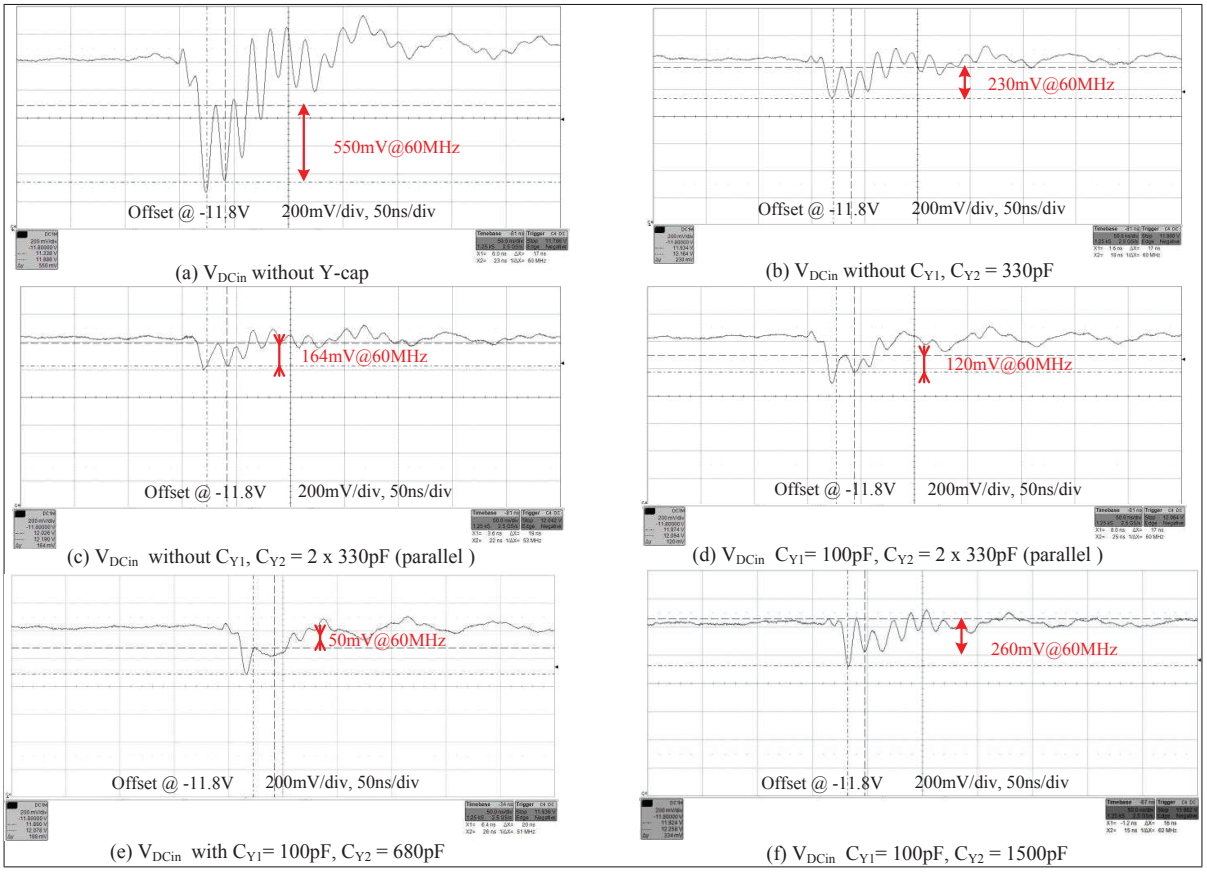


Figure 5.10 Experimental results of input voltage of DC/DC converter with/without proposed Y-cap

Therefore, the Y-caps are employed to attenuate the voltage oscillation at 60MHz. Several combinations of Y-caps are used, resulting in Figs. 5.10b-f. Amongst those combinations, the minimum oscillation, 50mV, at 60MHz is shown in Fig. 5.10e, where C_{Y1} and C_{Y2} are chosen as 100pF and 680pF, respectively. The results are explained by the Y-cap branch impedance Z_{CY} shown in Fig. 5.11 as follows:

First, the oscillation is reduced gradually from case (b) to (e) as shown in Fig. 5.10. This attenuation corresponds to the decreasing of Z_{CY} impedance at 60MHz shown in Fig. 5.11. It is also observed that the best attenuation performance is achieved at case (e) where the branch impedance consists of a positive phase the minimum amplitude.

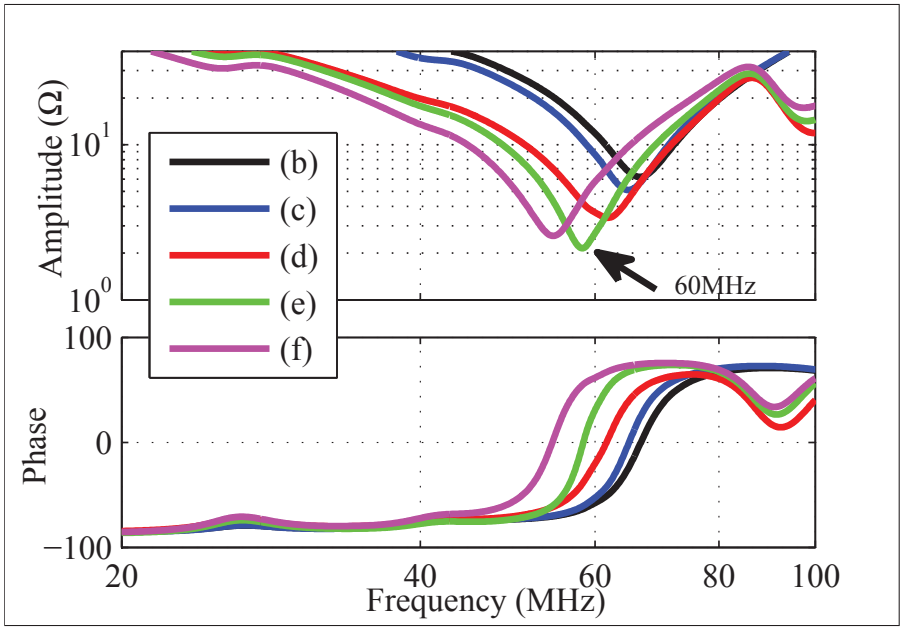


Figure 5.11 Branch impedance with proposed Y-caps

Second, the best performance is obtained at the optimal selection of Y-caps in term of capacitance value and number of capacitors. As seen in Figs. 5.10(b)-(d), the oscillation decreases with the increasing of the number of parallel Y-cap in such cases that Y-cap corner frequency is higher than the considered frequency. For example, the oscillation is reduced from 230mV (case (b), one 330pF capacitor) to 164mV (case (c), 2 parallel 330pF). Furthermore, employing C_{Y1} = 100pF in case (d) furthers reduces Z_{CY}, hence, reduces the voltage spike to 120mV. In addition, the same total capacitance can result in different spike attenuations, as observed in case (d) and (e), where the voltage spike are 120mV and 50mV according to the total capacitance of 660pF and 680pF, respectively. On the other hand, in case (f), C_{Y2} = 1500pF, which is much higher than 680pF, creates the 260mV oscillation at 60MHz, which is 520% of the optimal case. These results point out the importance of the corner frequency of the Y-cap and Z_{CY} branch, which must be correctly selected.

Third, the voltage oscillation at lower frequency, $f_g = 17$MHz is slightly reduced by the higher capacitance Y-cap as an observable trend in Fig. 5.10a to Fig. 5.10f. It opens the door to optimize Y-cap combination for good noise attenuation in both high and low frequencies.

5.5 Conclusion

In this chapter, the high frequency noise on the Gate driver DC/DC converter has been analyzed, and a practical method using Y-cap to provide noise attenuation has been introduced. Y-caps can be widely used due to their flexibility and low cost. The experimental results show the effectiveness of Y-caps by high attenuation for noise at very high frequency. The ability of Y-cap for noise attenuation purpose at lower frequency range and its optimal combination for working on both frequency ranges will be considered in a future work.

CHAPTER 6

DESIGN GUIDELINES FOR A LOW NOISE PROFILE - LOW POWER CIRCUIT

6.1 Overall power converter design procedure

As presented in Chapters 2 and 5, the origin of noise in low power circuit is voltage ringing on the power transistors during their switching transients. Once this noise propagates to the low power circuit, it creates voltage disturbance on the supply of functional circuits, degrading the converter reliability. In order to attenuate the noise level, several mitigation techniques are employed, as proposed in Fig.6.1. One observes the Y-cap utilization in the Gate driver to contain the high frequency noise. A filter and ferrite beads are placed between each DC/DC converter and the low power rails to increase the impedance paths seen from the gate driver. In addition, the decoupling capacitors are placed along the low power rails to further reduce noise traveling to functional circuits.

Even though the aforementioned parts of the low power circuit are studied in this thesis, noise profile prediction is still a difficult task due to the large model of each part of the circuit. Consequently, how to design a low noise profile converter remains a challenge for designers. To cope with this issue, one suggests an intuitive design procedure based on equivalent circuit background, knowledge of noise performance on change of the aforementioned separated components and practical experience.

This procedure is summarized as below and described in details in the remaining parts of this section.

- The schematic is design with the selected converter configuration and functional circuits for feedback, control, communication and protection. The next step is to design in PCB level.
- Complete routing of the high power circuit.
- Local placement and routing of functional circuits.

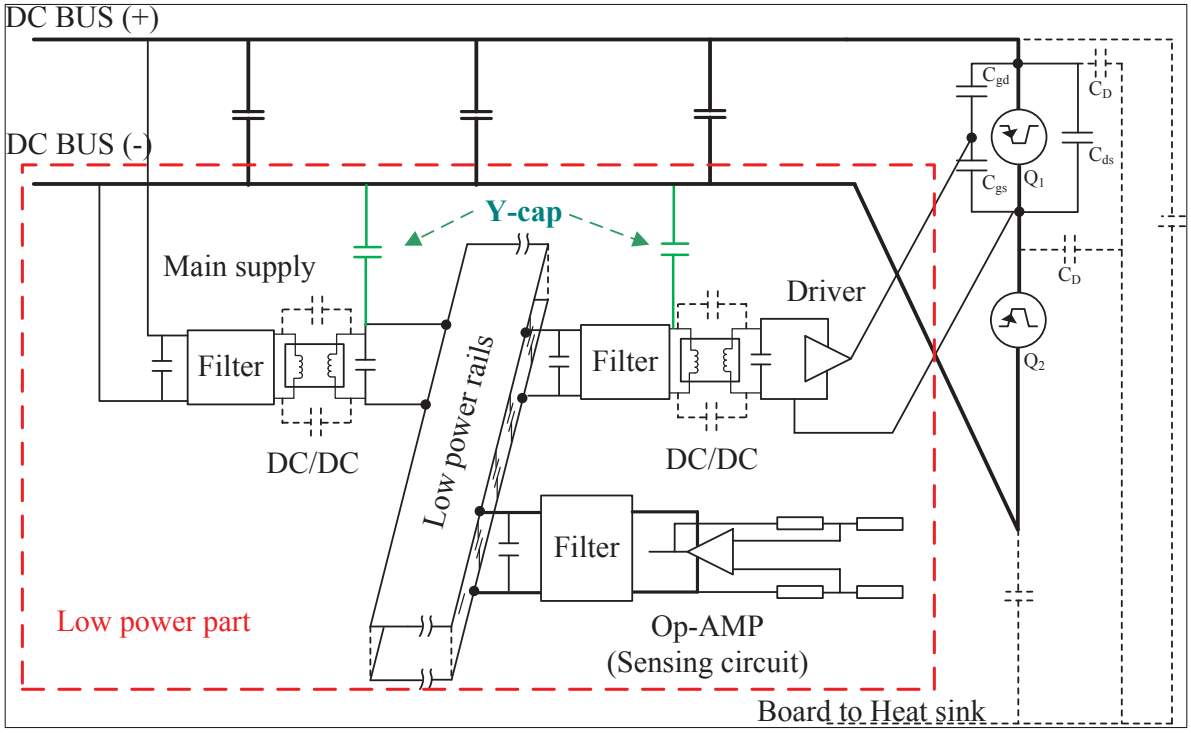


Figure 6.1 Complete design for low noise profile low power circuit

- Placement of all functional circuits on the PCB due to its functions. For instance, the current/voltage sensing circuits are placed nearby the current/voltage sensors; output of the controller is placed nearby the input of gate driver, etc. In this step, all functional circuits sharing the same power supply rails should be placed closed to each other to have easy access for the low power rails.

- The low power rails is designed to connect all functional circuits based on converter geometry and functional circuit locations.

- Finally, improve noise profile of the low power circuit. This task consists of several steps presented in the next sections.

6.2 Noise mitigation design procedure for low power circuit

6.2.1 Step 1 - Gate driver circuit design

As presented in Chapter 5, Gate driver circuit is the entrance of noise before propagating to low power circuit. Therefore, locally attenuating noise in Gate driver circuit is mandatory.

In this step, all decoupling capacitors in the low power plane are not placed, all the ferrite beads and filter are shorted. The low power circuit in this step is shown in Fig. 6.2. The converter is operated in open – loop to detect noise frequency ranges by measuring voltage oscillation at input of DC/DC converter supplying the Gate driver or current on low power rails, as presented in Chapter 5. Knowledge of these noise frequency ranges are mandatory to design the filter for functional circuits and Y-cap in the next steps.

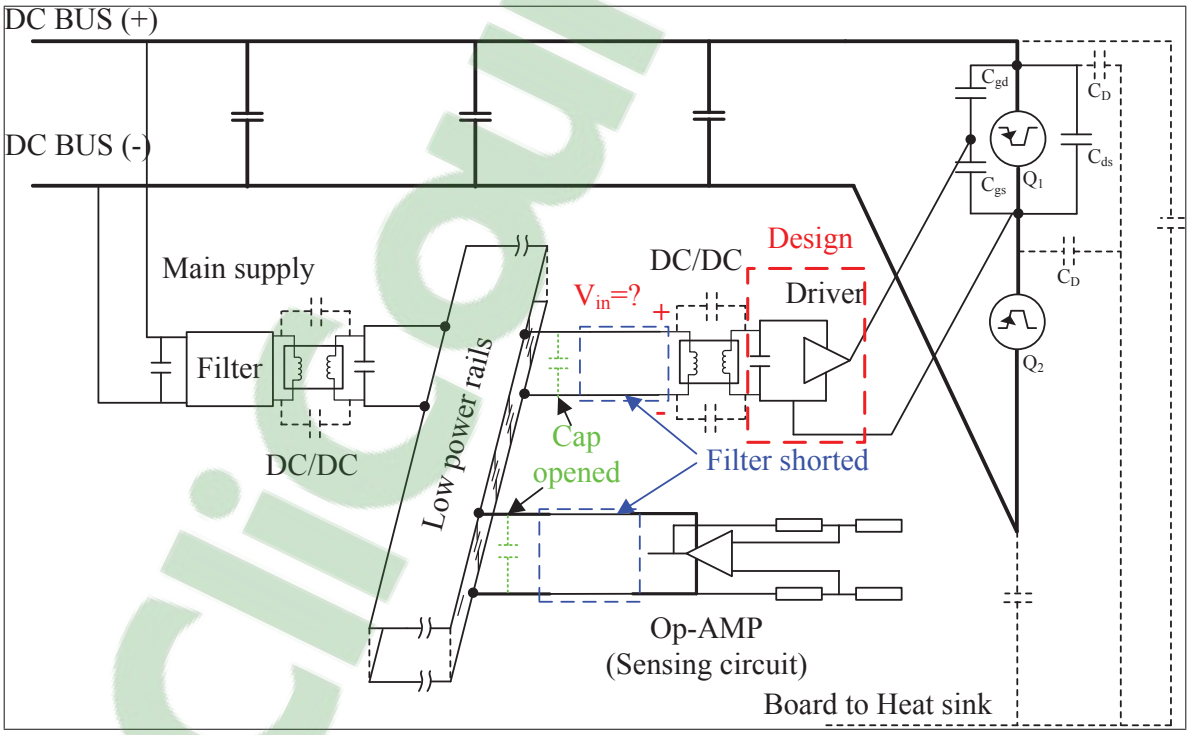


Figure 6.2 Step 1 of design process - design Gate driver circuit

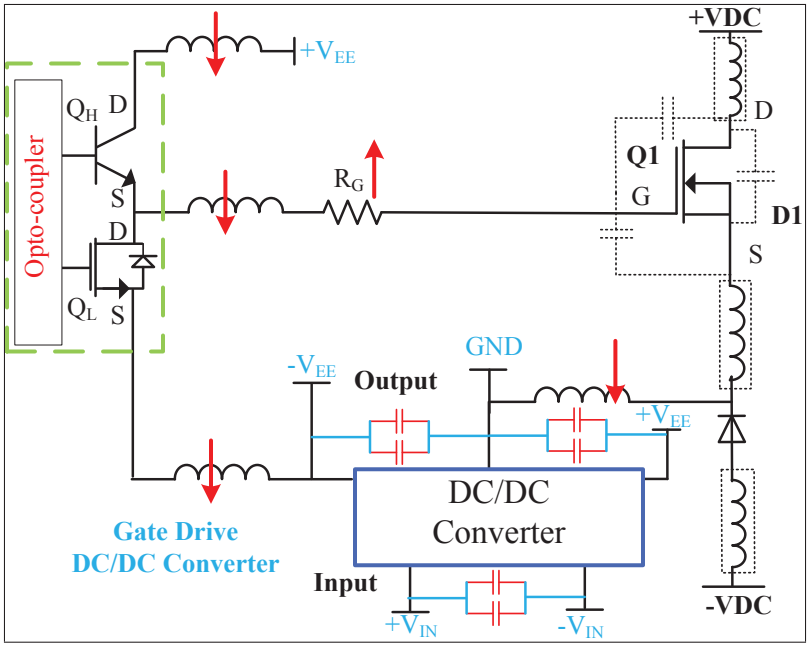


Figure 6.3 Detailed guidelines for design Gate driver circuit

Then, the Gate driver is designed based on the below guidelines which are also summarized in Fig. 6.3.

1. Maximize the gate resistor while satisfies the delay time at rising and falling edges of the power transistors required by the switching frequency and control strategy. The gate resistor acts as a damping resistor of the low power circuit, so that high gate resistance helps to reduce noise level.

2. Stray inductance between components in gate driver circuit such as opto-coupler, gate driver DC/DC and power transistors are minimized by creating as short returned path for current as possible for each component: placing the ground plane wherever it is possible, short and large traces, smallest component package as long as thermal requirements are satisfied.

3. Decoupling capacitors are placed at the input and outputs of the DC/DC converter according to the noise frequencies to provide the low impedance return paths. Also, decoupling capacitors are suggested to place at the supply of the Opto-coupler. For example, in ad-

dition to the usual $0.1uF$ capacitor, a parallel capacitor of a few nF is recommended to reduce decoupling impedance at high frequency.

6.2.2 Step 2 - Y-cap and Ferrite bead design

Once the major voltage/current spike frequencies f_d is determined, Y-cap and ferrite beads are used to noise at frequency of f_d by the method presented in Chapter 5 for each Gate driver. The Y-cap is employed to provide a low impedance return path Z_{CY} for high frequency noise at frequency of f_d to propagate to the high power circuit. In addition, high impedance of ferrite bead is added to increase equivalent impedance of the low power circuit seen from the gate driver (Z_{lpl}) at f_d, hence, it helps to reduce noise current propagating to the low power rails. The low power circuit in this step is shown in Fig. 6.4.

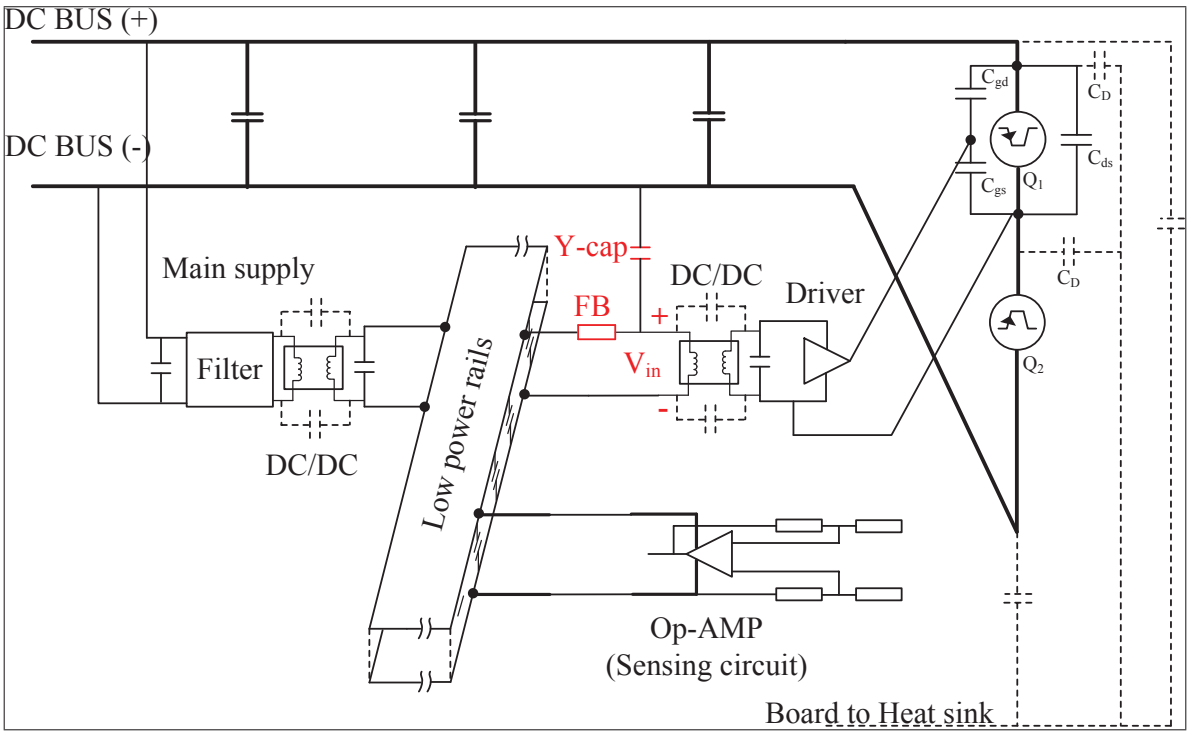


Figure 6.4 Step 2 - design Y-cap and ferrite bead

6.2.3 Step 3 - Filter design

6.2.3.1 Filter design for Gate driver circuit

The complete filter is recommended in Fig. 6.5a, where ferrite beads are designed at step 2 is added to the CLC filter configured by the common choke and two capacitors. The impedance model of this filter can be represented by GIR which is introduced in Chapter 3. Based on the VTG between pin pairs of this filter, the filter's components can be adjusted for optimal filtering function in the considered frequency range.

As experimental investigation in Chapter 2, DC/DC during its switching operation can be represented by its isolation capacitance. Therefore, the equivalent impedance of the Gate driver circuit including ferrite bead and input filter, seen from the low power plane, shown in Fig. 6.5a, can be replaced by the equivalent impedance of the filter and DC/DC converter isolation capacitance, as given in Fig. 6.5b. This equivalent impedance of the filter is computed by GIR. The voltage spike generated from the gate driver circuit is represented by a voltage source, resulting in the equivalent circuit shown in Fig. 6.5b.

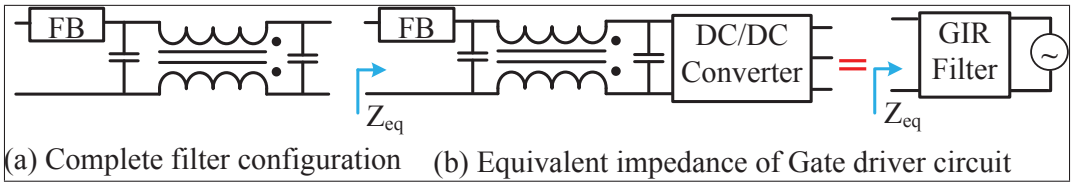


Figure 6.5 Step 3 - design filter for Gate driver

6.2.3.2 Filter design for sensing circuit

For typical power converter, voltage and current are measured by either isolated or non-isolated sensors. Depending on the sensor, its output voltage can be unipolar or bipolar. This output voltage is filtered and scaled before being connected to the DSC (for digital controller) or control ICs (for analog controller) using Op-AMP circuits. These Op-AMP are supplied by

unipolar or bipolar rails according to the sensor output voltage range. The supply rails for Op-AMP, typically +5V or $\pm 5V$ are converted from the +12V rail of the low power plane using LDO or discrete DC/DC converters. Taken into account the very low PSRR of Op-AMP, as discussed in Sec. 2.1, the power supply for Op-AMP must be filtered to avoid noise injection from the low power rails. Since significant noise is generated from the gate driver circuit, the filter for OP-AMP supply can be used as same as the filter designed at the input of gate driver, presented in Sec. 6.2.3.1. Due to high input impedance of Op-AMP, the equivalent circuit of the Op-AMP circuit is represented by the filter impedance. This equivalent impedance is used as the auxiliary impedance on the low power rails model.

6.2.4 Step 4- Low power rail design

Subsequent to local designs of all functional circuits such as gate driver and sensing circuits, the low power rails supplying all functional circuits is taken into account. Its layout is based on the converter geometry and the locations of functional circuit power supplies. The footprints of ferrite beads and decoupling capacitors next to the input of functional circuit supply devices are reserved. Also, the footprints of the decoupling capacitors are distributed along the low power rails. All decoupling capacitors are not populated since their values will be computed in later step. The model of the low power rails is created by the 2D-lumped model method introduced in Chapter 4. The GIR of the filters used in all functional circuits are employed as the auxiliary admittance matrix. At each location reserved for decoupling capacitor on the low power plane, the effects of each value of decoupling capacitor on VTG from the gate driver to the sensing and controller circuits are determined. Based on the results, the optimal decoupling capacitor value is selected at each location to minimize the mentioned VTGs at noise frequencies, which are detected in Step 1.

6.3 Conclusion

In this chapter, a design procedure to minimize noise in low power circuit of power converter is proposed. Detailed design guidelines for each part of low power circuit are suggested based

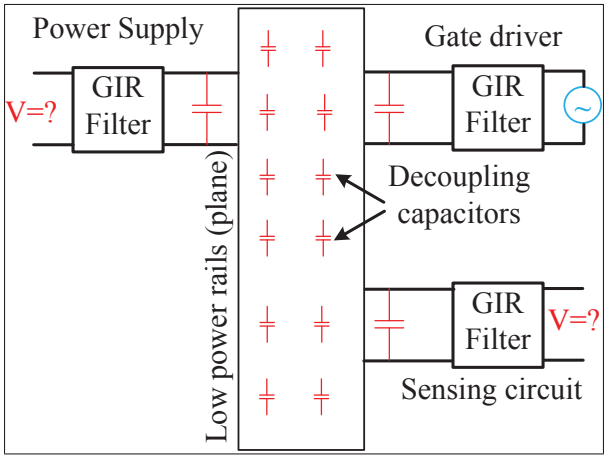


Figure 6.6 Step 4 - design low power plane

on practical experience and computational models introduced previously in this thesis. The advantage of the proposed design process is that each part is designed considering the equivalent impedance of the surrounding circuits. Consequently, impedance profile of the complete low power circuit is taken into account at the last step of the design process. It is useful for global noise mitigation without a heavy computational model of the complete low power circuit.

CONCLUSION AND RECOMMENDATIONS

Conclusion

This thesis has presented the noise issue in low power circuit, which has not been addressed in literature, in term of its origin, propagation principle, modeling techniques and attenuation approaches. Not only introducing new modeling techniques, but this thesis also provides the guidelines minimize noise in the low power circuit by optimizing design of fundamental parts. The suggested guidelines are issued based on researches of fundamental components, PCB structures and the gate driver circuit. Below are the conclusions of each part presented in this thesis.

In Chapter 2, experimental results of the noise spectrum in low power rails of a small scaled buck converter are introduced. As observed from the results, both CM and DM noise in low power rails increase significantly when the high power transistor is operating. They are the evidences showing the origin and propagation paths of the noise in low power rails, which is the main motivation of the research topic presented in this thesis. Furthermore, the current spectra are given with different operating points of high power circuit and component impedance of low power circuit. These results lead to other research topics which are presented in the following chapters.

The novel impedance models of general passive devices (Chapter 3) and low power rails structure (Chapter 4) are proposed. Each component is modeled as an impedance network, enabling them to be easily combined into a complete model to compute VTG in the low power circuit. Another important advantage of the proposed approaches is their generality. In case of GIR, it can be applied for all kinds of passive devices as black-box models regardless of their predefined models. In case of low power rails model, it is proposed for any kind of low power rail geometry and external device locations, providing flexibility for designing the low power rails in a typical power converter. The research also provides insights of these components on their effects on noise performance. It helps power converter designers to understand well component behaviors and give them ability to adjust design of components to improve the noise profile.

Moreover, the noise attenuation method for gate driver using Y-cap is introduced with proposed practical selection procedure in Chapter 5. It delivers the designers the noise origin and the reasons behind the design guidelines for gate driver. Even though Y-cap has been widely used in practical applications, but this is the first time it is used for the gate driver. Furthermore, this chapter provides the method of selecting Y-cap according to the leakage inductance of the power transistors, which has not been pointed before.

Recommendations

This thesis has focused on study of the fundamental components used in the low power circuit to release the practical power converter design guidelines for noise mitigation. However, the accuracy of complete model of low power circuit can still be further improved by taking into consideration other devices and PCB structures which have not been studied in this thesis. Furthermore, optimization procedure can be obtained from the proposed models. Some ideas for further development of this thesis are suggested below.

Develop an optimization approach for EMI attenuators in low power rails

In Chapter 4 of this thesis, the mathematical model to compute VTG in the low power rails considering its complex geometry and impedance of external devices is introduced. Based on this result, one can conduct the research on optimization to design low power rail geometry as well as EMI attenuator selection and placement. The optimization algorithm can focus on the EMI frequency ranges in which significant noise is generated due to switching transients of the power transistors, as presented in Chapter 5.

Develop a noise computational method based on discrete component models

In the PCB design, there are some areas that the power/ground plane can not be used due to constraints of voltage clearance or current capability. Thus, the PCB structure without current return path, which has not been studied in this thesis, usually appears. An important question arises at this point: “Is it possible to ignore these areas in VTG computational model or other modeling techniques such FEM or PEEC must be used?”. To answer this question, one needs to

build a computational model for the complete circuit by integrating the models which are presented in this thesis together. The VTG different level between computation and measurement will provide interesting information about this issue in any case. In case the error is negligible, the model in this thesis will be able to apply for automatic optimization design. Otherwise, the new research topic will be opened to consider the new PCB structures.

Develop new computational technique for connectivity devices

Usually, the low power circuit is connected to the high power circuit at the common points such outputs of current/voltage sensors, gate driver signals via headers and connectors. In motor drive applications, it is connected to the encoder measuring motor speed by cables. The connections via headers, connectors or cables can have impact on CM noise propagation in the low power circuit, further significantly contribute on noise profile. One should develop an computational method for these connections utilizing FEM or PEEC methods and integrate them into the full noise prediction model of the low power circuit. Based on the results, one can choose the optimal connecting configurations for noise minimization purpose.

APPENDIX I

LOW POWER RAILS EQUIVALENT CIRCUIT

The power rails with power/ground planes structure is a two-port reciprocal network which can be represented by an equivalent circuit, is shown in Fig. I-1. The transfer gain from Port A to Port 0 can be obtained by:

$$VTG_{A,0} = \frac{V_0}{V_A} = \frac{Z_L Z(1,2)}{[Z_L + Z(2,2)]Z(1,1) - [Z(1,2)]^2} \quad \text{(A I-1)}$$

where Z_L is the load impedance which is 50Ω in experiment; $Z(1,1)$, $Z(1,2)$, $Z(2,1)$ and $Z(2,2)$ are elements of impedance matrix $[Z]$ which is computed as Pozar (2009).

$$[Z] = ([I] + [S])([I] - [S])^{-1} Z_0. \quad \text{(A I-2)}$$

where $[S]$ is the scattering matrix, $[I]$ is the 2×2 identity matrix and Z_0 is the reference impedance.

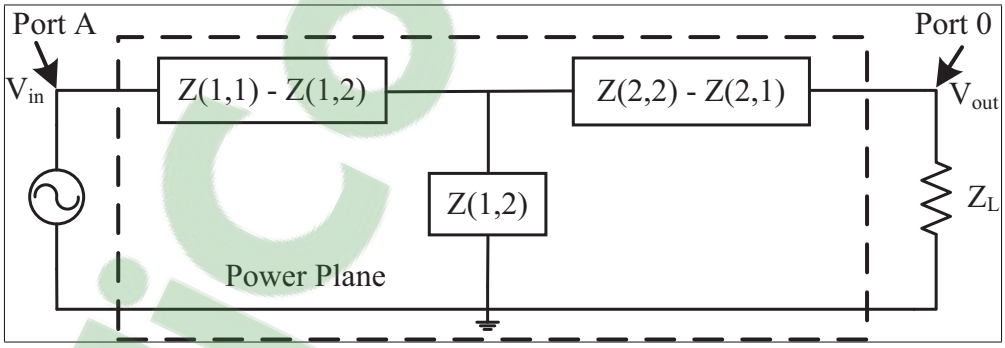


Figure-A I-1 Equivalent circuit of power rails

APPENDIX II

S-PORT CALIBRATION PROCEDURE

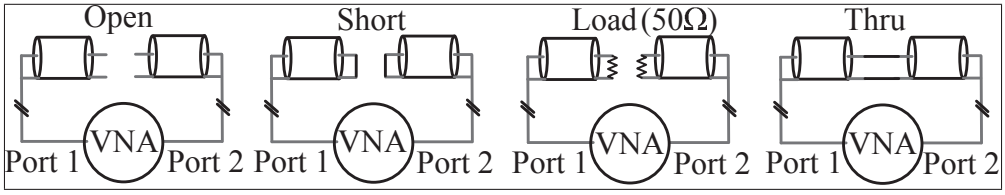


Figure-A II-1 Calibration procedure of a two - port VNA

To remove the effect of cable impedance, the S- port calibrations, i.e. open, short, load and through, must be performed at the end of the cables, as depicted in Fig. II-1.

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